Основною особливістю запропонованого методу розпізнавання зображень є синтез неявно виражених визначників, які описують не тільки критерії, що роз'яснюються фізично, а також і ті, які не можна описати за допомогою простих фізичних розмірностей. Тобто такі визначники описують будь-які опосередковані інтегровані комбінації стандартних величин.

KVP-перетворення мають велику перспективу використання в різноманітних системах, в яких необхідно здійснювати розпізнавання об'єктів (пошуку, стеження, діагностування, контролю та ін.).

1. Кожемяко В. П., Тимченко Л. И., Лысенко Г. Л., Кутаев Ю. Ф. Функциональные элементы и устройства оптоэлектроники. К., 1990. 2. Кожемяко В. П. Применение оптоэлектронных логико-временных сред в информационно-вычислительной технике. – К., 1988. 3. А. с. СССР № 1119035, МКИ G 06 G 7/14. Способ параллельного сложения длительностей группы временных интервалов./ В. П. Кожемяко, Л. И. Тимченко, Т. В. Головань //Открытия. Изобрет. 1984. № 38. 4. Кожем'яко В. П., Понура О. І., Кожем'яко О. В. Універсальний спосіб генерації визначників для неалгоритмичного розпізнавання зображень та реалізація його на логіко-часових середовищах //Вимірювальна та обчислювальна техніка в технологічних процесах. № 2, 1997. С. 13–19. 5. А. с. СССР № 1101817, МКИ G 06 F 7/50. Устройство для сложения./ В. П. Кожемяко, Л. И. Тимченко, Т. В. Головань, Н. Е. Фурдияк //Открытия. Изобрет. 1984. № 25.

УДК 681.32

Wlodzimierz Kalita, Jerzy Potencki
Rzeszow University of Technology, Department of Electronic Systems

PROSPECTS IN DEVELOPMENT OF VOLUME MICROELECTRONICS STRUCTURES

© Wlodzimierz Kalita, Jerzy Potencki, 2000

Contemporary development trends in technology of integrated circuits have been presented especially taking into account a role of third dimension for increase in integration scale and functional possibilities of ICs.

Розглянуто сучасні тенденції розвитку технології інтегральних схем, особливу увагу приділено ролі тривимірних структур, які дозволяють збільшувати масштаб інтеграції і функціональні можливості інтегральних схем.

1. Introduction

In 1896 year Guliemo Marconi sent the first telegraph signals through air, and almost simultaneously, Aleksander Popov transmitted the first radio messages. In 1901, the first and regular radio communications across the Atlantic were established. These were very important dates. However, in the common opinion, the date of born of modern electronics, is assumed the year 1904, when John Ambrose Fleming created the tube diode, the first electronic element. In 1906, Lee de Forest built the first amplifier and in 1912, Edwin Armstrong constructed the first non-mechanical oscillator. The next epoch-making step was made in 1928 year when John Baird transmitted TV signal over the telephone lines. Two years later the first picture and sound was sent in the same manner. The next revolutionary step was made in 1947. It was the invention made by

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

Shockley, Bardeen and Brattain, the first transistor. In relatively short period of time, the next pace was made. In 1958 year the Texas Instrument made the first integrated circuit (IC) and three years later, Intel Corporation prepared the first commercial IC. We waited only 10 years for the adjacent significant invention. In 1972, Intel Corporation constructed the first microprocessor. It is a very briefly presented history of the electronics development. Many of the important dates and facts have been neglected here.

Since these dates the hundreds of thousands of integrated circuits, microprocessors, and other electronics elements have been elaborated and millions of different electronics equipment have been manufactured. Every day the fabricated equipment is more compact, smaller and lighter, operates in higher frequencies, and consumes less and less power. Unnoticeably, the electronics, at the end of 20th century has entered the all areas of human life (telecommunications, entertainment, automotive, computers, military, avionics, medical, etc.). At present, daily life without electronics in civilised world is totally unimaginable.

2. Miniaturisation problems

From the first days of electronics up today, the greatest challenge faced by the electronic industry is the ongoing demand for smaller feature sizes in active electronics assemblies. This process is often called "scaling". Scaling simply refers to the drive to continue making the transistor, and technology that connects transistors together, smaller. As a transistor becomes smaller, it becomes faster, conduct less electricity and finally, it also consumes less power. Example of this activity is MOS transistors, being the base element of modern integrated circuits. The critical dimension of a MOS switch, first introduced about 15 years ago, has gone down from 10 microns to less than 0.2 microns in leading chips today. In that time, chip's electrical frequency rate has also increased by more than 50 times, and the number of the transistors on the chip has gone up by a factor of 20 [13].

From the above mentioned facts it can be concluded that the most important factors of modern electronics development are its miniaturisation, increase of the operating frequency, and tendency to reduction of dissipated power.

2.1. Printed Circuit Board

The demands of "faster-smaller-cheaper" and the responses have motivated the electronics industry into a revolution. Perpetual progress in semiconductor industry brought more power and more problems. Chips with millions of transistors needed 1000 and more I/O connections to the outside world. Consumers demanded portability for converging technologies The interface between the IC and circuit board was to be made. The electronics package was under severe pressure to shed girth.

The ever-downsizing package was quickly running out of real estate with its peripheral wiring scheme and micro-pitch leads were becoming an assembler's nightmare. The salvation was Packaging Revolution, that was launched when area array designs, like Ball Grid Array (BGA), became a major focus. Chip on Board (COB), Flip-Chip on organic circuits and new Chip Scale Packages (CSP) also became part of the shrinking landscape. But the Packaging Revolution puts extraordinary demands on the circuit industry for higher and higher density. That pulls electronics industry right into the next stage of domino effect, the Printed Circuit Board (PCB) Revolution.

They are currently produced using the some subtractive and additive methods. The first one is usually connected with etching process. The other ones are based on additive or buid-up

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

methods. Conductors then are deposited on dielectric using the several different techniques (painting/printing, spraying, chemical deposition, vacuum deposition, die stamping, dusting, etc.).

The two areas for circuit densification are conductor line width/spaces and vertical interconnects. Both areas are receiving considerable attention, with impressive government and industrial funding. General solutions for not enough density of classical one- or two-sided PCB are currently the multilayer boards with inside vertical connections. The original plated through-hole process, launched in 1953 by Motorola (Placir Process), is replaced by process structures that are more efficient. Drilling is being replaced by lasing and plasma etching. The plated through-hole is replaced by direct plating through micro-vias. Build-up multilayer methods have become commercial where holes are photodefined. Interposer methods, where anisotropic conductive adhesives mate circuit pairs together, are also enjoying successes [1, 2].

2.2. Coupling Characteristics

The evolution of modern electronics in the third-dimension generates a series of new computation, technological and design problems on one hand, and on the other one allows the realisation of a new class of electronic devices and systems (systems with thermal feedback, distributed RC networks, microstriplines, etc.). In the second case couplings give possibilities of an adequate forming of circuit parameters, i.e. feedback, synthesis of functional devices, etc.

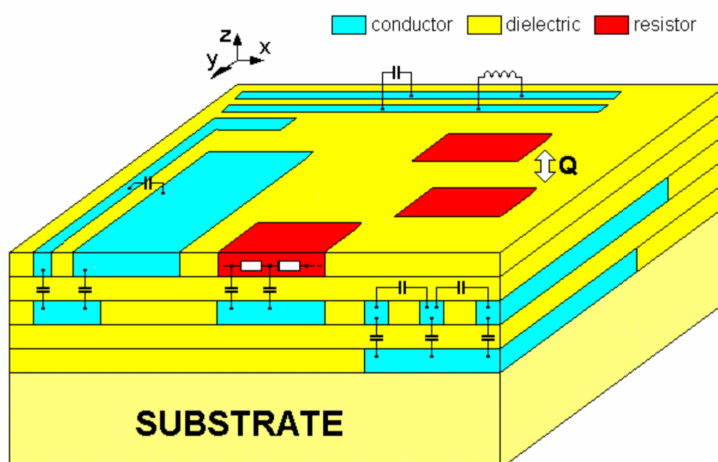

Fig 1. General view of multilayer structure and systems of internal couplings

The main problems of these types' circuits manufacturing are related to the presence of series of inter-elements' couplings (electrical and thermal). They are exceptionally strong in multilayer circuits, due to extremely small distances between particular elements (from few to several tens micrometers), good thermal conductivity of substrate and relative high density of dissipated power. They modify action of microcircuit in the full frequency range - from fraction Hz to GHz. Their influence increases with growth of frequency and applied power. In the range of low frequencies, the galvanic and thermal influences are important. For higher frequencies significant role play both capacitive and inductive ones.

2.3. Thermal Problems

Short looks in the history of electronics teach us the following: when vacuum tubes were replaced by transistors, the power consumption dropped drastically. The power dissipation in tubes was usually much more than the power delivered to the load. The introduction of the transistors changed completely the power requirements of electronics circuits. First, of all, transistors operate

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

at much lower voltages and do not need any heating for thermionic emission. The integrated circuits with several, thousands and then millions transistors on one chip came after the transistors. Packages were getting smaller, circuits packed closed together to meet the requirements for higher operating speeds. All these facts increased the power density, so that at present the thermal problems are more severe than in the good days of vacuum tubes. For example, the 486 chip several years ago consumed less than 5 Watts, while a Pentium consumes about 10 Watts, and a 400-MHz Pentium II has peak power consumption of about 28 Watts.
Taking into account the above data, chip's surface, total number of transistors on chip and their dimensions, one can calculate that a dissipated power density per unit volume reaches the value of $10^{16}W/m^3$. This is certainly an incredible high number and probably the highest power density on earth.

3. Multilayer Interconnection Systems

Network fabrication is accomplished by patterning metals and dielectrics onto a free-standing substrate to form the base of a microcircuit. A variety of substrates, processes, and metals are used to do this. Several options are available for producing networks depending on the requirements for circuit size, heat produced, operating frequency, cost and other factors. The universal solution was the development of multi-chip module (MCM) technology.

The simplest definition of a multichip module is that of a single electronic package containing more than one IC. Based on this simple definition, the MCM combines high performance ICs with a custom-designed common substrate structure, which provides mechanical support for the chips and multiple layers of conductors to interconnect them. This arrangement takes better advantage of the performance of the ICs than does interconnecting individually packaged ICs because the interconnect length is much shorter. The really unique feature of MCMs is the complex substrate structure, which is fabricated using multi-layer ceramics, polymers, silicon, metals, glass ceramics, laminates, etc. Thus, multichip modules are not really new. They have been in existence since the first multichip hybrid circuit was fabricated. Conventional PCBs utilising chip-on-board (COB), a technique where ICs are mounted and wire-bonded directly to the board, have also existed for some time. However, if packaging efficiency (also called silicon density), defined as the percentage of area on an interconnecting substrate that is occupied by silicon ICs, is the guideline used to define the MCM, then many hybrid and COB structures with less than 30% silicon density do not qualify as MCMs. In combination with packaging efficiency, a minimum of four conductive layers and 100 I/O leads has also been suggested as criteria for MCM classification [1].

A formal definition of MCMs has been established by the Institute for Interconnecting and Packaging Electronic Circuits (IPC). They defined three primary categories of MCMs, which are designated as MCM-L, MCM-C, and MCM-D.

MCM-L: Modules which are constructed of plastic laminate-based dielectrics and copper conductors utilising advanced forms of printed circuit board technologies to form the interconnects and vias. With state-of-the-art line, width and spaces can be small as 50□m. They are commonly called "laminate MCMs" [5-12].

MCM-C: Ceramic based MCM-C can be built using three different approaches: thick-film, low-temperature co-fired (LTCC) and high temperature co-fired ceramics (HTCC). In the thick-film case, standard thick-film technology is used, but with insulating pastes, which have relative dielectric constant between 2.5 and 4. Using fine resolution print techniques, conductor lines

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

100μm wide are used to produce a substrate with controlled impedance lines. In the co-fired case, regular low or high temperature co-fired technology is used. Again, the only modification is that a green tape with low dielectric constant is applied.

The term "co-fired" implies that the conductors and ceramic are heated at the same time. LTCC and HTCC networks are produced using screen-printed conductors and resistors on multiple layers of green ceramic tape. Up to 80 layers of ceramic can be printed and then co-fired for high-density networks. An advantage of this process is that the network produced forms a microcircuit package that can be sealed. These are also called thick film MCMs [3-9].

MCM-D: Modules that are formed by the deposition of thin film metals (aluminium, copper or gold) and dielectrics, which may be polymers or inorganic dielectrics (alumina, aluminium nitride, diamond, silicon, etc.). These are commonly called thin film MCMs. The layers in these type of structures, can be deposited in the thermal evaporation processes (filament, electron beam), vapour sputtering (DC, RF, magnetron sputtering), electroplating and electroless plating. In addition to sputtering and evaporation, there are other methods of dielectric materials depositing. There are plasma enhanced-low pressure-chemical vapour deposition (PELPCVD) and photoinduced CVD. A major advantage is the precision patterning consistent with higher frequency circuits [5-10].

It is important to note that these are simple definitions. Consequently, many IC packaging schemes, which technically do not meet the criteria of any of the three simple definitions, may incorrectly be referred to the MCMs. However, when these simple definitions are combined with the concept of packaging efficiency, chip population, and I/O density, there is less confusion about what really constitutes the MCM. The fundamental (or basic) intent of MCM technology is to provide an extremely dense conductor matrix for the interconnection of bare IC chips. Consequently, some companies have designated their MCM products as High-Density Interconnect (HDI) modules. From the above definitions, it should be obvious that MCM-Cs are descended from classical hybrid technology, and MCM-Ls are essentially highly sophisticated printed circuit boards, a technology which has been around for over 40 years. On the other hand, MCM-Ds are the result of manufacturing technologies that draw heavily from the semiconductor industry.

The MCM technology is an emerging solution for the electronic packaging, facilitating the interconnections and reducing the electrical length between devices, which contributes for the minimisation of propagation time, crosstalk, and attenuation of signals. Although MCM techniques offer many performance advantages, the cost is the main factor limiting mass production.

For MCMs of any type, special attention must be paid to methods of heat removal without excessive temperature rise. In very special cases, quite new methods such as change-of-state cooling or liquid immersion may be considered, but in the majority of applications, conduction is the primary method of heat removal. For improvement of heat conduction, the series of new filling inter-element space materials have been elaborated. The modern systems of heat distribution create the multilayer three-dimensional systems also. In some cases, thermally conductive vias additionally penetrate the entire thickness of the substrate. In very special cases, a Joule-Thompson cooler can be built into the substrate.

4. IC development

Most of today's integrated silicon products were once a group of single-chip modules on a board several years ago. As functional design progressed and silicon integration advanced, it

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

became possible to put many circuits onto the same chip and receive the benefits of lower cost and higher performance. Not only can this circuit integration be done sooner with MCM technology, but also many things, which appear too difficult or expensive, can be done. This would include mixtures of analog and digital devices that cannot be integrated, ultra high-performance functions, which cannot be supported in silicon yet, and, perhaps, some high-power components integrated with digital silicon.

It seems the concept of development and modification of planar technologies, that could be possible manufacturing of chips with multilayer structure to be more prospective in practical applications. Currently manufactured ICs have a two-dimensional structure. It means that localisation of particular elements on the silicon substrate can be defined by the two coordinates, x and y. The turning-point in this area, step in third dimension, promise the series of works on the elaboration of manufacturing technologies of thin mono-crystalline layer on the insulating substrate. It makes prospective fabrication of ICs in a typical "sandwich" form, when crystalline silicon layer (consisting of transistors and diodes} are separated each from the other by a thin isolating layer. The practical achievement of this goal is very difficult due to material and technological reasons. Concepts of such circuit construction and its application are schematically presented in Fig. 2 and 3, respectively.

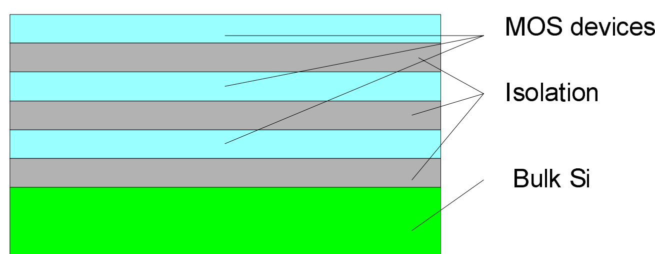

Fig. 2. Concept of multilayer ICs manufacturing

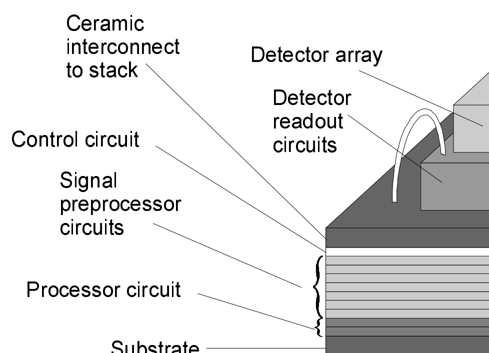

Fig. 3. Example application

4.1. SOI technology

One example of this prognosis of practical fulfillment is, currently introduced by IBM into mass production, the novel solution of SOI (Silicon on Isolator) technology. SOI refers to placing a thin layer of silicon on top of an insulator such as silicon oxide or glass. The transistors would then be built on top of this thin layer of SOI. The basic ideas are that the SOI layer will reduce the capacitance of the switch, so it will operate faster, and increase the circuit density. This conception was born in the early 1970's [13].

The silicon film used for making MOS transistors is perfect crystalline silicon. The insulator oxide layer on the other hand is not crystalline. It is very difficult to make perfect crystalline silicon on oxide or silicon with other insulators since the insulator layer's crystalline properties are so different from pure silicon. If perfect crystalline silicon is not obtained, then defects will find their way onto the SOI film. This could degrade the MOS switch severely both in terms of speed and leakage through the switch. One insulator found to be perfectly crystalline and whose properties are close to those of silicon is sapphire. There are a number of methods, part of them under development, for making suitable SOI materials and wafers. They will be widely developed in the near future. Example of these type chips has built and tested by IBM. They have produced 20-25% cycle time and 25-35% improvement over equivalent bulk CMOS technology. This is equivalent to about two years of progress in bulk CMOS technology (Fig. 3).

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

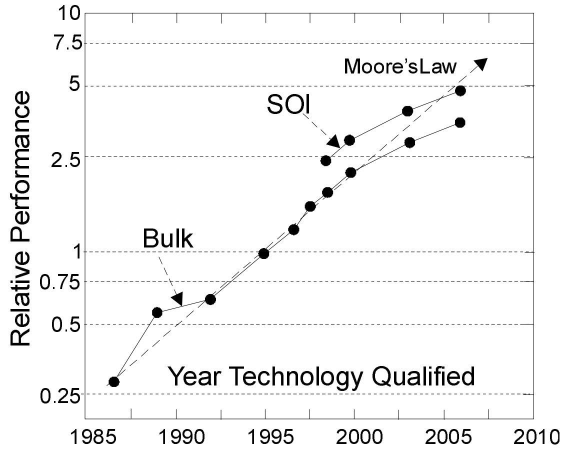

Fig. 4. Plot of bulk and SOI transistors relative performance. Elaborated on the Moor law

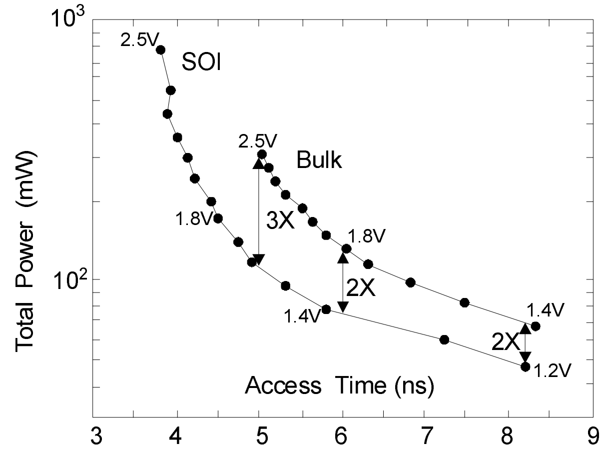

Fig. 5. Performance characteristics derived in lab tests using SOI-based chips

4.2. Molecular Beam Epitaxy

One of the most exciting and useful developments in modern semiconductor electronics is capability of engineering band structure, quantum phenomena, optical properties, and other useful effects by the growth of multilayer heterostructures. With the development of advanced semiconductor devices growth techniques such as molecular beam epitaxy (MBE) has been observed.

In MBE, metallic sources of Ga, Al, and As, along with dopants Be and Si, are evaporated or sublimed from individual ovens into ultra-high vacuum chamber and direct onto surface of GaAs wafer held at about 600^0C. The epitaxial growth rate is about one monolayer per second, and shutters in front of the various sources can be opened and closed on the time of monolayer growth. As the result, precisely controlled layers of GaAs an AlGaAs can be grown in one single crystal form on the lattice material.

The availability of high-quality multilayer heterostructures has led to new effects having widespread applications such as two-dimensional transport effects, quantum wells, modulation doping, delta doping, carrier and photon confinement, etc. As final result of these capabilities of advanced crystal growth, the future for new device invention and development is extremely fertile, combining electronic and photonic effects in new ways for novel applications [14].

5. Conclusions

As long as we can make the transistors smaller and faster, make the wiring that attaches them less resistive to electrical current and make each chip denser, the digital revolution will continue to accelerate into the 21st century. Development of the conventional manufacturing technologies of the ultra scale integration ICs slowly reaches the saturation state. New technologies based on the quantum-, opto- and bioelectronics, achieve in the 21st century areas and levels of microelectronics evolution hard definable today. The technological niches create, however, big sphere of activities for technologies in which, third dimension creates possibilities for practically unlimited growth of ICs functional properties. The possibilities of scientific activities of universities and research institutions in our countries in this area should been seen.

1. Leonida G.: Handbook of Printed Circuit Design, Manufacture, Component & Assembly, Electrochemical Publications Ltd., Ayr, Scotland. 2. Gilleo K.: The Early and Fascinating History

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua

of The Printed Circuit, Alphametals Inc. 3. Brown R.: Microwave Hybrids, A Technical Monograph of ISHM, Reston, 1991. 4. Gilleo K.: A New Multilayer Concept Based on Anisotropicity, Proceedings, NEPCO WEST, Anaheim, Feb. , 26, 1990. 5. Fursman J.: Advanced Interconnect - The future of the Hybrid Industry, Proc. of the 8th European Hybrid Microelectronics Conference, Rotterdam, 1991, pp. 425-433. 6. Harper Ch.: Multichip Modules (MCMs): Market Analysis and Technology Trends, SMTnet, 1999. 7. Harper Ch.: Electronics Packaging & Interconnection Handbook, SMTnet, 1998. 8. Stoller H.: Multichip Modules: A Technology in Your Future? IBM MicroNews, Vol. 2., No 4. 1998. 9. Vrana M., Van Calster A., Vanden Berghe R., Allaert K.: Interconnection Technology for Advanced High Density Thick Films, Proc. of the 10th European Microelectronics Conference, Copenhagen, 1995, pp. 190-198. 10. Barnwell P.: Alternative Interconnection Technologies - A personal View, 5th European Hybrid Microelectronics Conference Proceedings, Stressa, Italy, May 22-24, 1985. 11. Val Ch.: 3D-interconnection applied to microsystems, Proc. of the 11th European Microelectronics Conference, Venice, 1997, pp. 133-139. 12. Cyrusian S.: Electrical Properties of Thin Film Multilayer Wiring Systems: A Comparison between Polyimide and PCB, Proc. of the 10th European Microelectronics Conference, Copenhagen, 1995, pp. 288-293.. 13. SOI Technology: IBM's Next Advance in Chip Design, IBM materials, 1999. 14. Streetman: Molecular Beam Technology, http://www.ace.utexas.edu/projects/ece/mrc/groups/ mbe.html 15. Ćwirko R., Rusek M., Marciniak W.: Układy scalone w pytaniach i odpowiedziach, WNT, W-wa, 1987.

УДК 621.382

О.З.Готра
ДУ "Львівська політехніка", кафедра інформаційно-вимірювальної техніки

ВЕРИФІКАЦІЯ ТЕМПЕРАТУРНИХ МОДЕЛЕЙ ЕЛЕМЕНТІВ ТЕРМОСЕНСОРНИХ ІС

© О.З.Готра, 2000

Розглянуто алгоритм верифікації температурних моделей p-n переходів транзисторних структур, що використовуються як первинні перетворювачі термосенсорних біполярних інтегральних схем. У процесі верифікації моделей ППП "Spice" можливе досягнення невідповідності між ними та характеристикою реальних структур ІС в межах (-0,8...0,7)% в температурному діапазоні (-50...+100)^{0}С.

The algorythm of verification of temperature models of p-n transistor structures that are used as primary transducers of thermosensitive bipolar integrated circuits is shown. In the process of verification of models of "Spice" it is possible to achieve the noncorrespondence between them and characteristic of real structures of IC in the range of (-0,8...0,7)% in the temperature range of (-50...+100)^{0}C.

Формулювання задачі

Процес дослідження температурних характеристик вузлів первинного перетворювача та оптимізація його режимів роботи повинні передбачати розробку математичних моделей елементної бази. Такі моделі, спільно з аналітичними та експериментальними дослідженнями, дозволяють підвищити ефективність розробки термосенсорних ІС, зокрема проводити

Lviv Polytechnic National University Institutional Repository http://ena.lp.edu.ua