Modeling of Threshold Voltage in Three-Dimensional SOI-Structures

Kogut I.T., Scherbyak V.M.

Abstract - **This paper proposed an original approach to the analysis of the threshold voltage metal-oxide-semiconductor structures based on local three-dimensional SOI-structures.**

Keywords - **SOI MOS-transistor, threshold voltage, three-dimensional SOI-structure, П-shaped profile gate, cylinder shaped gate.**

I. INTRODUCTION

Due to increased interest and potential to three-dimensional SOI-structures to create the element base of LIC and microsystems-on-chip actual approaches to mathematical analysis and modeling of their parameters. An original approach to the analysis of threshold voltages and drain currents of MOS-structures based on local three-dimensional SOI-structures is proposed. The distribution of potential and electric field in underchannel field of SOI MOS-transistors and their influence on the formation conduction (inversion) channel with different profiles of three-dimensional gates is analyzed.

II. METHOD OF MANUFACTURE OF LOCAL THREE-DIMENSIONAL SOI MOS- TRANSISTOR STRUCTURES

Formation of a local three-dimensional SOI MOS-transistor structures were made by developed method [1,2] using the processes of modern industrial CMOS-technology manufacturing integrated circuits, thermal oxidation, deposition of silicon nitride films, isotropic and anisotropic plasmachemical digestion et al., directly from the original wafer material that ensures their high crystalline perfection. On the basis of three-dimensional SOI-structures, three-dimensional forms of SOI MOS-transistors which are different from the traditional have been developed.

Moreover, the proposed method can generate local three-dimensional SOI-structures, namely the areas which isolated from crystalline silicon wafers of silicon oxide formed at a given depth under the surface of the wafer in the cavitys and also on this base create integrated circuits and microsystems-on-chip, including three-dimensional SOI-transistors (Fig. 1), for which method of calculating drain currents and threshold voltages is suggested.

III. METHOD OF CALCULATION OF THRESHOLD VOLTAGE.

To simplify the calculation of threshold voltage of SOI MOS-transistors with three-dimensional configuration of the gate it was asked to consider them as separate single-gate and parallel connected transistors formed on a horizontal, vertical walls and angular segments of the body of the transistor.

Two transistors in the vertical side walls will have equal threshold voltage, because their geometric and electrophysical parameters are symmetrical. (Fig. 1)

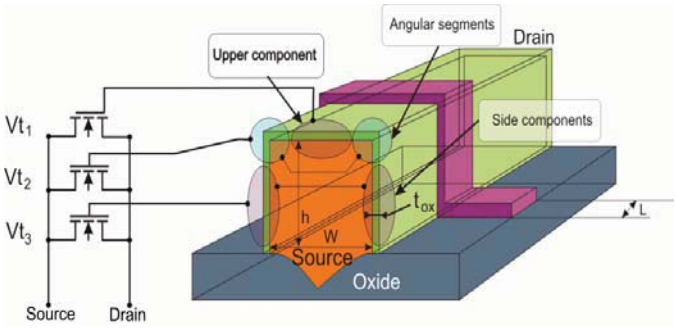

Fig. 1. Structure and equivalent circuit diagram of three-dimensional SOI MOS-transistor for calculating drain currents and threshold voltages.

When the output of the analytical expression for the three-dimensional transistor threshold voltage in general, keep in mind that it will be equal to the smallest threshold voltage of all three transistors that are considered, ie:

$$V_T=\min(V_{T1}, V_{T2}, V_{T3}) \quad (1)$$

Manufacturing real three-dimensional transistors does not allow to get a strictly rectangular body of the transistor, so the slightly rounded corners should be taken into account to calculate threshold voltage. These areas form another pair of transistors, which are also connected in parallel with the three previous ones. In essence, rounded shape of the body angle is indefinitely large number of elementary transistors connected in parallel, each of which will have its threshold voltage.

IV. CONCLUSIONS

A method of the analysis of drain currents and threshold voltages for three-dimensional MOS-transistors based on local SOI-structures was proposed. The analysis by this method and simulations provide a good match. That can be used in the design of integrated SOI-devices with three-dimensional architecture.

REFERENCES

[1] І.Т. Когут, В.І. Голота, А.О. Дружинін, С.В. Сапон, Пат. №36463 Україна. Спосіб виготовлення локальних тривимірних структур «кремній–на–ізоляторі»; published 27.10.2008. – Bulletin №20.

[2] І.Т. Когут «Локальні КНІ- структури – перспективний матеріал для інтегрованих мікросистем-на-кристалі» Прикарпатський вісник НТШ (Фізика і хімія твердого тіла). №1,-2008. pp. 164-172.

[3] І.Т. Когут, А.О. Дружинін, В.Т. Голота, «Архітектура і елементи інтегрованої мікросистеми на базовому матричному кристалі зі структурою кремній-на-ізоляторі» Вісник НУ ЛП, 2008, №646, pp.86-95.