Research outputs cascades of CMOS gate array with silicon-on-insulator structure

Kogut I. T., Dovhij V. V.

Abstract: **In this paper research output cascades for integrated circuits and microsystems-on-chip with silicon-on-insulator structures (SOI) of executed after traditional CMOS process and with the use of double control by connecting to the subchannels areas in SOI MOS transistors.**

Keywords: **gate array, output cascade, silicon-on-insulator structure, SOI CMOS inverter.**

I. INTRODUCTION

When designing the output cascades important are accouunts of such parameters as their speed, consumable power and area on a crystal. Traditionally for designing output cascades use 4-stage CMOS inverter, which provides good stepness fronts of impulses and large loading ability. However the lacks of such technology are delays of output signals, unoptimum area on a crystal and large power consumption. SOI structure due to possibilities of double control subchannel erae opens the possibility of designing new circuit solutions with improved perfomance. Use of these benefits is show in example output cascades for integrated circuits (IC) and microsystems-on-chip on gate array with SOI structures.

II.TECHNOLOGY OF OUTPUT SOI CMOS GATE ARRAY CASCADES CONSTRUCTIONS

For research of characteristics was designed two types of output cascades and their topologies. The first from them is executed after traditional CMOS technologies with SOI structures (Fig. 1, a), and the second type of output cascade is based on the use of double control a subchannel area in SOI CMOS transistor (Fig. 1, b). Second type combines advantages of small consumable power, which is characteristic of SOI CMOS structures and high speed of and promoted loading ability, which is advantage of bipolar structures [1].

III.RESULTS OF RESEARCHES

The circuits design on a direct current and tranitional descriptions shawed that output cascade on the basis of incorporated bipolar and SOI CMOS structures has substantial advantages comparatively with 4-stage SOI CMOS signals creator [2]. Transitional characteristics of these cascades showed on Fig. 2.

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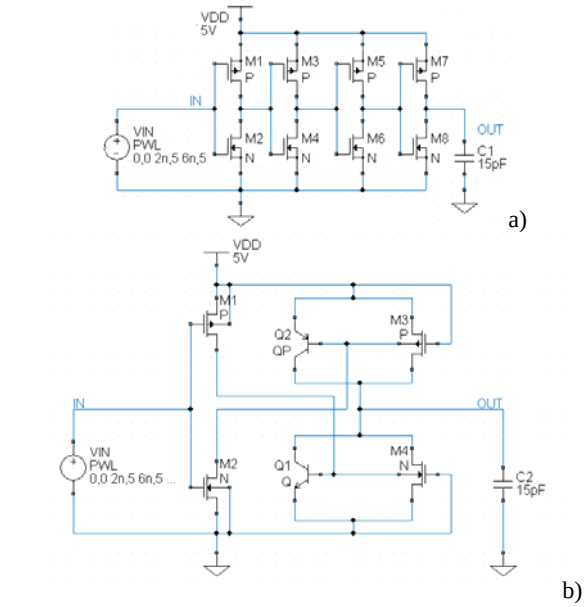

Fig 1. Electric circuits of output cascades: a) executed after traditional SOI CMOS technology; b) with the use of double control the areas of subchannels in SOI CMOS transistors.

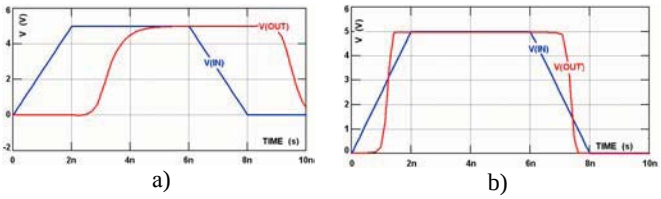

Fig 2. Transitional characteristics: a) 4-stage SOI CMOS cascade; b) SOI BiCMOS output creator of signals.

IV. CONCLUSION

As evidently from the results of researches, output SOI CMOS cascade has substantially greater speed of switching as compared to 4-stage SOI CMOS inverter. In addition, consumable power of buffer SOI CMOS cascade approximately on 40% below, than in 4-stage SOI CMOS inverter at the identical capacities of load capacitance.

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