The Principles of Traffic Processing and Formation Based on IXA Networking Processors

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Abstract – **The paper presents network processors architecture and services, describes the use of network processors in the devices of traffic processing and formation.**

Keywords – **Network processor, Internet Exchange Architecture.**

I. INTRODUCTION

One of the key challenges for telecommunications is the task to minimize losses and increase income with simultaneous provision of new services. Service providers need network equipment with not only high performance, but also flexibility, which would allow adding new paid services according to the way they will adjust the networks to new standards. In meeting these requirement, of particular importance are programmed network processors since the focus is on the packets processing speed, and here the entire job is done by active elements of network infrastructure – routers, switches, access nodes, and other devices participating in formation of traffic in packet networks.

II. TRAFFIC PROCESSING AND FORMATION DEVICES MAIN COMPONENT

Each network level requires a peculiar combination of performance, features, and expenses. In order to be efficient, network processors must be optimized not only with view to particular requirements as to the equipment, but also with the account of services which are provided in each network infrastructure segment.

In accordance with network development, the network processors performance shall depend more and more not only on performance, but even more on the intellectual processing of the packets at speeds commeasurable with transfer speeds. To provide paid services, the providers will have to combine performance and flexible control over resources. For instance, a data transfer channel with 10 Gbit/second requires perfect check-out of packets with interval of 35 nanoseconds. Network processor should perform necessary applications, and then transfer them without losses, in correct sequence and at required speed.

The Intel network processors architecture is a perfect solution to this problem, providing a highly efficient platform programmed by the equipment manufacturers to implement new algorithms of data processing. Multi-processing sub-system of 2G network processor guarantees the availability of aggregated computing power sufficient for processing packets coming at the speed of 10Gbit/second.

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Besides, new Intel processors maintain packets stream analysis to solve such issues as splitting the router operation into several successive tasks which include receipt of packets, reference to routing tables, and packets classification. Thanks to the performance and flexibility ensured by this data processing programmable pipeline, the processor can simultaneously perform several tasks while taking into account the relationship between time and data.

2G network processor architecture includes implementation of unique technology – Hyper Task Chaining of Intel corporation, which allows to split one stream of packets into several successive tasks, which easily link to each other. Memory register technology allows splitting the signals of data and events between the streams and microengines virtually without delays, ensuring their consistency. One more new development – Ring Buffers – maintains interaction between microengines using FIFO principle, implementing highly efficient mechanism for flexible distribution of tasks between different software pipelines. Thanks to the combination of flexible software pipeline processing and fast communication between the processes, Hyper Task Chaining technology allows Intel IXA network processors to perform complex data processing at the speeds of data transfer.

III. CONCLUSION

Therefore, the network processors are the key element of information network equipment. Their key function is to ensure processing and distribution of information packets coming from different network devices according to routing table. The ability of network processors to be programmed allows equipment developers to create additional services for users by recording additional program blocs into the existing devices.

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