Features of Forming Sub-Micron Gaas-Structures on Schottky Field-Effect Transistor (SFT)

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Abstract – **This article describes a problem about small Schottky barrier height for p-channel GaAs field-effect transistors complementary pair.**

Keywords – **Gallium arsenide, GaAs, Schottky transistors, field-effect transistor, integral circuits.**

I. INTRODUCTION

One of the main problems is small Schottky barrier height for p-channel GaAs field-effect transistors complementary pair.

II. RESULTS

In association with the fact that the manufacture self-combined SFT refractory material used as the shutter mask in the multiple ion implantation, Schottky contact must withstand the following heat treatment (including fast), which is already needed to activate implanted impurities. It was this work carried out research on the impact of different types of heat treatment on high-rise Schottky barrier, which formed Schottky contact with the tungsten nitride (WN) to p-GaAs.

Obtained for diodes made dependent barrier height and diode factor n from the annealing temperature, held after magnetron deposition of WN for n-and p-channel SFT shown in Fig. 1. The originality of this technology is that of tungsten nitride as a barrier was deposited high-frequency magnetron sputtering tungsten target in a nitrogen plasma on the installation of “Oratorio-5”. For this first experiment used multiple implantation [1].

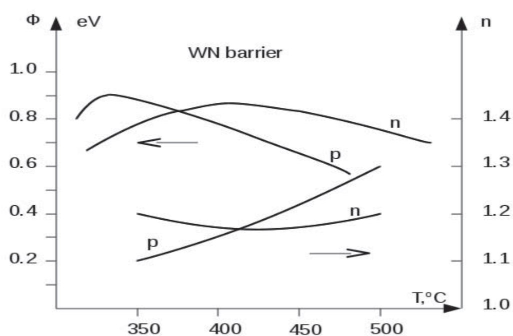

Fig.1. Dependence of barrier height Φ and diode factor n for n- and p-channel SFT

Stick-turn region have formed multiple implantation of magnesium (Mg^{++}) with energy 70-80 keV and dose (1-2) 10^{13} cm^{-2}. That is, we got value for the SFT barrier at 0.68-0.71 eV in the largest diode coefficient n = 1.4 ± 0.15.

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Besides using the PSPICE simulation was carried out valves, as shown in Fig. 2. It is interesting to note that gates c) and d), which are diodes for level shift will increase the voltage from 0.7V to 1.2V. But Gates b) and d) are complementary, because he-channel transistor has been using depleted.

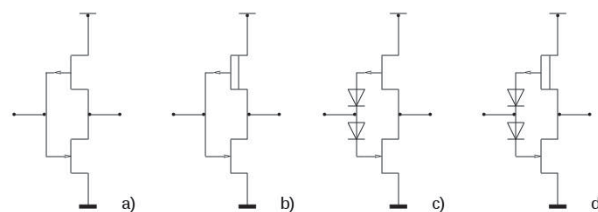

Fig.2. Test logic elements that are subject to modeling the performance

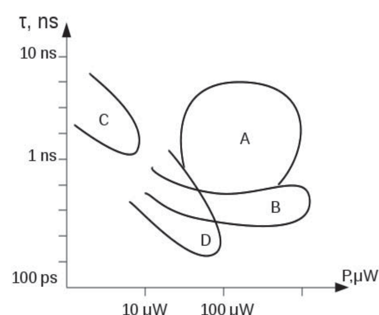

Fig.3. Dependence of speed logic gate a, b, c, d, depending on power consumption

The simulation results are presented in Fig.3. τ - Time delay; P - power that dissipated by gate; A, B, C, D - respectively correspond to the gates a), b), c), d) on Fig.2.

III. CONCLUSION

Thus, studies of test structures allow to conclude that Gates (inverters), which formed on the basis of base pairs of SFT using semi-combined bolt of tungsten nitride and multiple implantation can be used for the formation of high-speed digital GaAs structures to replace silicon LSI.

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