Simulation Model of Delta-Sigma Modulator

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The segment of precision ADC is filed by the converters based on delta-sigma modulator (DSM). Such ADC are in the line of leading companies and are very popular on the market. These ADC have highest parameters but there are many applications which demand more precision converters. The example of this task is precision resistance measurement using replacement method. There the main signed component of instrumental error is proportional to integral nonlinearity of ADC's transfer function (TF). Therefore accuracy improvement for this application demands nonlinear component of error correction. For example, 24-bit ADC type AD7714 has integral nonlinearity not more than 15 ppm, and it correspond to 16-th bit. In the same time its effective resolution is up to 22 bit. So the nonlinearity of TF is 6 low signed "effective" bits or 8 LSB (taking the noise into consideration). So nonlinearity correction is actual task.

Some methods provides precision identification the integral nonlinearity of ADC's TF in the set of testing points [1,2]. But the implementation these methods for correction of nonlinear error of ADC demand forming interpolation curve for whole range. So the task of the presented work is oriented on investigation the character of TF's nonlinearity of ADC based on DSM for providing adequate forming the interpolation curve.

The existed models of DSM does not provide investigation of dependence of view and parameters of interpolation curve vs parameters of DSM's components. Therefore there was developed simulation model, which consist DSM as the linear combination of nonlinear components and provide access to parameters of these components.

The structure of single bit single cascade DSM is presented on fig.1. It consist of forwarding signal and backwarding signal channels. The first of them consist of adder – –, integrator – and synchronous comparator – C (which consist of asynchronous comparator and synchronous D-triger – TT). Backwarding signal channel consist of single bit digital to analog converter – DAC, which is controlled by output code of DSM. Synchronization pulses for trigger TT is generated by clock generator – G.

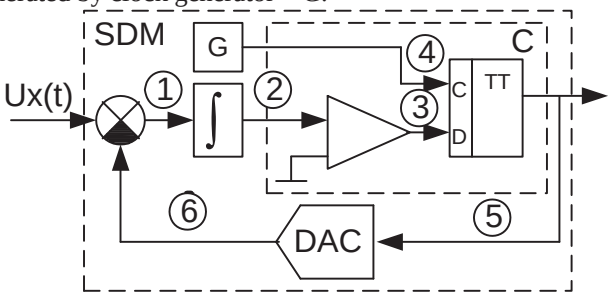

Fig.1. Structure of single bit single cascade DSM

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The voltage of points 1…6 of fig.1 - $U_1 \dots U_6$ vs time t are the component equation of simulation model. The topologic equation of linearized model of DSM could be presented as the system of equations

$$\begin{cases} U_1(t) = U_X(t) - U_6(t) \\ U_2(t) = \dfrac{1}{\tau}\int_0^t U_1(t)dt \\ U_3(t) = \begin{cases} 1, U_2(t) > 0 \\ 0, U_2(t) \le 0 \end{cases} \\ U_4(t) = \begin{cases} 1, t \in [k \times T, (k+0{,}5) \times T] \\ 0, t \in ((k+0{,}5) \times T, (k+1) \times T) \end{cases} \\ U_5(t) = \begin{cases} U_3(t), (U_4(t) = 1) \wedge (U_4(t - \Delta t) = 0) \\ U_5(t - \Delta t) \end{cases} \\ U_6(t) = \begin{cases} E, U_5(t) = 1 \\ -E, U_2(t) = 0 \end{cases} \end{cases}$$

where: U_X - input voltage; τ - characteristic time of integrator; T - period of clock generator; k - integer value; $\Delta t \to 0$ - modeling time step; E - reference voltage of DAC.

The conversion result n

$$n = \sum_{i=l}^{l+N} U_5(i \times T)$$

where : $N = 2^K$ - maximum number of voltage discretes of ADC, which is defined by resolution K; $l = \frac{t1}{T}$, where $t1$ - time of attainment of integrator to the operation mode.

For investigation the influence of components' parameters on the modulator's parameters the output signal of appropriate component is shifted. The value and sign of this shift is defined by value of parameter. The simulation model is oriented on analysis in time domain and implements the approach of asynchronous incrementing simulation with constant time step. This model is implemented using C++.

The final manuscript consist some results of developed model verification and results of investigation of influence of components' parameters on error components for single bit single cascade DSM.

REFERENCES

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