Tools for micro-satellite video stream compressing

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The features of constructing devices in modern FPGA for lossless compression of video stream by JPEG-LS method and CCSDS121.0-B-2 recommendation are considered in detail.

Keywords: lossless compression, FPGA, JPEG-LS, CCSDS121.0-B-2, software implementation, hardware implementation.

Introduction

The paper considers the features of lossless compression of video stream using CCSDS121.0-B-2 recommendation [2] and JPEG-LS method [1], as well as their implementation in the FPGA. The lossless compression method eliminates the redundancy of the data source, and after decoding it can completely restore compressed data. This method is especially useful when the integrity of the data should not be violated [5].

In the work the complexity of lossless video stream compression devices are compared.

Structure of the data compression unit according to CCSDS 121.0-B-2 recommendation

The source encoder for lossless compression consists of two distinct functional parts: a preprocessor and an adaptive entropy encoder.

The preprocessor function is a reversible operation, and, in general, the best Lossless preprocessor will produce the lowest entropy, which is a measure of the smallest average number of bits that can be used to represent each sample.

The function of an adaptive entropy encoder is to calculate uniquely encoded words of variable length that correspond to each block of data coming from the preprocessor. The entropy encoder implements several encoding options, each of them is effective for different entropy ranges of input data. The encoder chooses the encoding option that gives the highest compression ratio for each of the block of input data. Since the number of block may be small and the best compression method is used for each block, generally encoding can adapt to rapid changes in data statistics.

Fig. 1 shows the functional diagram of generally accepted adaptive entropy encoder along with a preprocessor. A unique identifier (ID) is added to the compressed data to indicate to the decoder necessary decoding method.

Realization of the CCSDS121.0-B-2 recommendation in the FPGA

The compression recommendation CCSDS121.0-B-2 is used in hardware implementations aimed at space exploration. One of the successful implementations is the core (IP Core) of the AMBA™ FPGA manufacturer[2]. Below is a structure (Fig. 2) and a description of each implementation component.

In the previous step, three basic operations are performed for each input sample according to core operation mode in the following order: formation of the feature of the extension of the previous block, formation of the predicted value of the subsequent data, and, finally, generation of filling for the last block of data flow (if necessary).

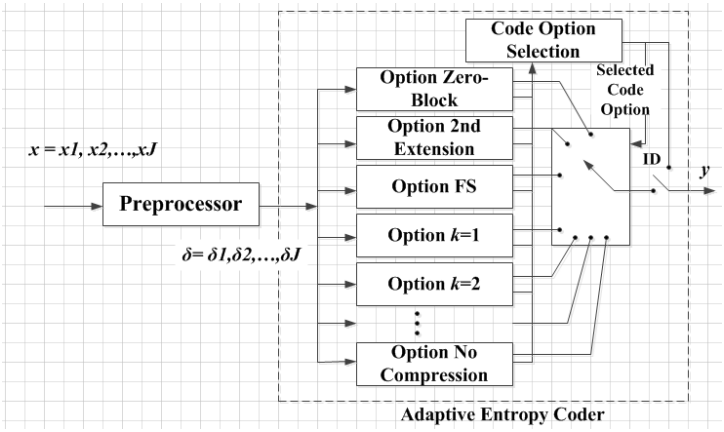

Fig.1 Adaptive entropy encoder with preprocessor according to CCSDS 121.0-B-2 recommendation

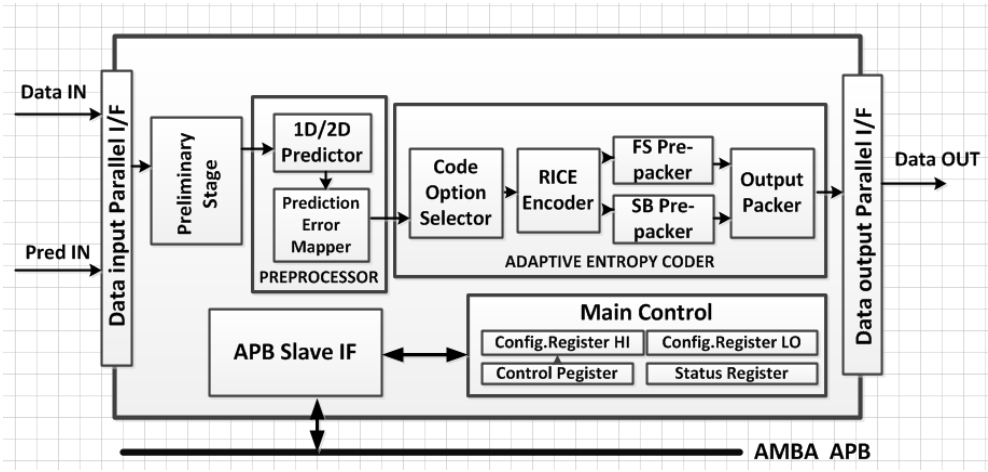

Fig.2 AMBA™ CCSDS 121.0-B-2 FPGA core structure

In the preprocessor unit there is a prediction unit that converts the value of prediction errors in non-negative integers.

Prediction Error Mapper takes the value of the prediction error and converts it in non-negative numbers suitable for Adaptive Entropy Coder.

The adaptive entropy encoder (AEC) has the following characteristics: a) the possible size of the block of data (J) is 8, 16, 32 or 64; b) it supports the basic or limited set of code parameters; c) its sample interval (r) is from 1 to 4096. These parameters are configured by the user through the configuration register.

The coding option selection unit simultaneously calculates the effect of using each of the compression methods and chooses the method that gives the highest compression ratio among the others same data block.

The RICE Encoder unit implements the basic Rice adaptive encoding algorithm that selects the best of several code options for use in the data block J.

Pre-Packer module is used for each of the FS (Fundamental Sequence) and separated codewords data streams as a pre-formatting processing step for each block of data. This way, the FS and split-bit codewords are pre-formatted and output on a 16/32 bit bus.

The variable-length Fundamental Sequence (FS) code represents the non-negative integer m with a binary codeword of m zeros followed by a 1. Application of the FS code to a block of J samples produces a sequence of J concatenated codewords called the Fundamental Sequence. Fig.3 illustrates the FS codewords.

Preprocessed Sample Values, δ_i	FS Codeword
0	1
1	01
2	001
.	.
.	.
.	.
2^n-1	0000 … 00001 (2^n-1 zeros)

Fig.3 Fundamental Sequence Codewords As a Function of the Preprocessed Samples

The Output Packer receives and multiplexes already pre-generated FS codes and separated bits from FIFO at the Pre-Packer output and outputs the finished CDS (Coded Data Set) packages to the 16/32-bit bus.

JPEG-LS

JPEG-LS lossless compression method is less variable in the choice of compression parameters than the standard described above [4]. Below is the structure of the FPGA core (Fig. 4) and a description of its components.

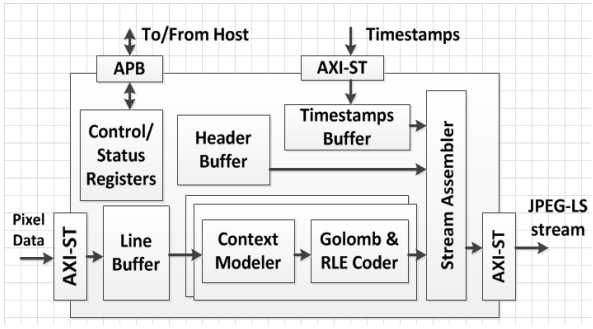

Fig.4 AMBA ™ FPGA core structure

The input buffer (Line Buffer) consists of a memory module and controls memory operations of reading and writing. This component stores input sample data that are fed to the core by the interface.

The Context Modeler module performs prediction error calculations. It accesses the line buffer output and reads four contextual values needed to define the context. In addition, this module performs middle forecasting procedures, finds the edge of the image and calculates forecasting error. Finally, this module updates the context-sensitive variables with new values of the statistical parameters of the selected context.

The Golomb Coder encoding module generates a Golomb code due to a prediction error and compression parameters.

Status/controls registers contains 4 16-bit status registers, as well as registers of control. The registry file performs operations for reading the state registers and the write control operations.

The described implementation can be taken as the basis for the creation of hardware implementations of special-purpose compression.

Capabilities of Vivado package (Xilinx) for conversion JPEG-LS algorithm C-description to suitable for implementation in FPGAs VHDL-description were tested and described in [5]. Also C language structures, which can not be processed by specified means and possible circumvention of such structures were defined.

Comparison of the hardware FPGA implementation characteristics of the JPEG-LS method and the CCSDS 121.0-B-2 recommendation

The characteristics of the hardware implementation of both compression methods are not very different. The difference in speed or volume of used memory can be seen in Table 1:

Table 1

	JPEG-LS [3]	CCSDS 121.0-B-2 [6]
Type of FPGA	Kintex -7	Virtex 5
Bits per pixel (max)	16	32
LUTs	5600	5809
Msamples / sec	180	175

Further research direction

In further development of microsatellite FPGA video stream compression unit it is planned to use the obtained analysis results and the advantages of both compression methods to create a FPGA-based lossless compression implementation that best suits customer requirements.

To accomplish the task, the following steps are planned:

• Based on the example of the structure of the FPGA encoder core for compression of images, to develop own implementation for compressing the video stream from microsatellite scientific information collection system.

• Explore the characteristics of the model of the developed system.

Conclusions

In this work the methods for lossless compression CCSDS 121.0-B-2 and JPEG-LS and characteristics of their implementation in the FPGA are investigated. Also, a comparison of the characteristics of their existing hardware implementations is performed. Results of these studies are planned to use in further development of video streams lossless compression FPGA core for microsatellites scientific data collecting system.

References

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