УДК 612.396

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PATH DELAY FAULT COVERAGE IN PSEUDORANDOM TEST SEQUENCES

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1. Introduction

Testing the operation of digital logic circuits requires verification of functional behavior as well as its operation at the desired speed [1]. This last issue corresponds to the problem of delay faults (called also AC faults). Delay faults relate to random variation in circuit production processing parameters or to aging and environment stress (e.g. temperature) effects. In delay testing two fault models are used: gate delay and path delay. The first model fails to deal with distributed defects that consist of small delays on many gates and wires. The second model is more universal, it detects localized and distributed delay defects. Hence we concentrate on path delay fault models.

Detection of a delay faults requires two pattern test vectors. The first pattern initializes some state on the input of the sensitized signal propagation path (comprising potential fault) and the second pattern realizes signal transition along this path. Fault identification is realized by direct time measurement or indirect evaluation of the result (e.g. correct operation at the system level). Many approaches has been proposed for generating path delay tests ([2,3,5,11,12] and references). Relatively good results were achieved with generators based on BDDD diagrams. In our Institute such generator has been developed and enhanced with various additional capabilities useful in testability analysis [11]. Direct application of test pattern pairs for all faults is cumbersome due to large cardinality of test sets. Moreover in system testing quite often we base on classical DFT and BIST circuitry which operate effectively especially for pseudorandom test patterns [4,9]. Hence arises the problem of checking their coverage for path delay faults.

To deal with the formulated problem we have analyzed properties of path delay test sets (section 2) and then checked fault coverage in many experiments. For this purpose a special program has been developed. This problem was neglected in the literature except a few papers [3,7,14] dealing with some specific issues e.g. special BIST and DFT circuitry for path delays which is quite different approach to that discussed in the paper. Section 2 of this paper gives an outline on path delay test generation and presents the problem of test execution in the system environment. Test coverage problems are discussed in section 3.

2. Path delay tests

Path delay tests are defined for a set of potential faults in the circuit as a set of test pattern pairs <v1, v2>. Each vector element can assume the following values 0, 1, -. A single path sensitization hazard free robust test is a pair of vectors that assures signal propagation via path such that it is free from dynamic hazards. In this case delay detection does not depend upon delays of the rest of the circuit. Robust test is analogous to the previous one except that it does not guarantee lack of dynamic hazards. Test that do not fulfill robust test requirements are called non

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