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NEIGHBOURHOOD PROBLEM IN INTERCONNECTION CAPACITANCE MODELING

Описано особливості моделювання VLSI схем на основі точних аналітичних моделей взаємних ємностей. Результати моделювання таких схем з урахуванням впливу сусідніх ліній дають можливість оцінити величину затримки сигналу та рівень перехресних спотворень від кількості паралельних ліній.

Modern VLSI circuits become more and more complex. For simulation purposes (especially statistical simulation) simple but precise analytical models of interconnection capacitances are necessary. Existing models take into account only the closest neighbourhood of the line. This paper presents example results of simulations showing that number of the parallel lines taken into account influences accuracy of signal delay and crosstalk evaluation.

1. Introduction

In modern technology the complexity of integrated circuits is very large and increases. Area of chips grows and circuits include millions of transistors. Effects occuring in interconnections, such as delay and crosstalk, become very important and often determine performance of the device.

Interconnection line may be represented by the net of parasitic elements: resistances, capacitances and inductances. They are responsible for signal delay and crosstalk between lines. In many cases the influence of inductance may be neglected [1, 2]. It allows the line to be modeled with RC-elements only. Such model will be assumed in the following.

Resistance of the line practically depends on its dimensions and resistivity of the material. Measured values of this parameter usually are available in the specification of the technology. However capacitances depend not only on the dimensions of the line itself but also on the configuration of other elements (such as other lines) in its neighbourhood. So the values of capacitances must be evaluated for different configurations of the lines.

Precise numerical computer programs (such as CAPCAL [3], FastCap [4-6]) allowing evaluation of the capacitances are available. Unfortunately numerical procedures are very time consuming and not useful for simulation of very complicated circuits. Especially statistical simulation, when the computations have to be repeated many times in Monte Carlo loop [7]. So simple and precise analytical capacitance models are necessary.

Till now several empirical capacitance models have been presented [8-12]. They allow evaluation of capacitances for two main structures in VLSI: parallel lines on one plane and between two planes (fig. 1). Although a bus may include many interconnection lines those models take into account only the closest ones. Our earlier considerations indicates that for lines between two planes (fig. 1.b) only the influence from the closest neighbours is really important [13]. That is causedby the planes, which intercept flux from the further lines. However in the case of one plane (fig. 1.a) neglecting further lines influence introduces errors. In fig. 2 values of capacitance

between the line and the plane Caf for different number of lines on one plane evaluated with empirical model [12] and with numerical extractor are compared. Depending on the number of lines numerical results change. Analytical model doesn't allow taking this effect into account. In effect achieved deviation using this model is different for different interconnection lines configurations.

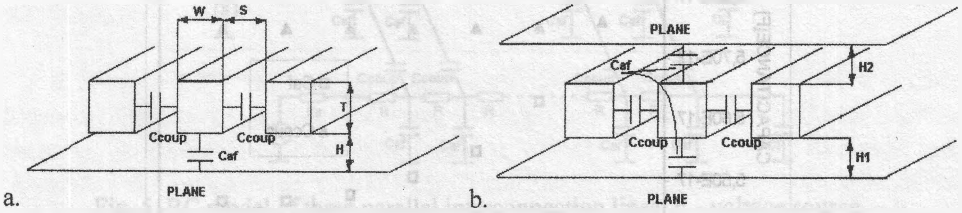

Fig. 1. Parallel lines on one plane (a) and between two planes (b). Ccoup - capacitance between lines, Caf -capacitance between line and plane

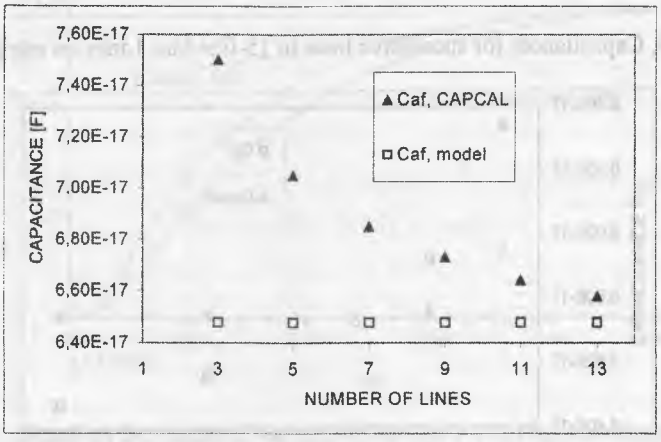

Fig. 2. Caf for middle line in the bus for different number of lines in the bus (T=S=H=W=1μm) from empirical Wong's model [12] and numerical extractor CAPCAL. Lines on one plane

In section II influence of further lines on the values of capacitances of interconnections are presented, basing on the results of numerical simulation. In section III changes in performance of the line caused by differences in configuration of further interconnections are shown. In the end we present conclusions.

2. Capacitances of parallel lines

For the computations numerical extractor CAPCAL [3] has been used. Values of capacitances for parallel lines on one plane (fig. 1.a) for different number of lines have been evaluated. Example results for lines dimensions: width 0.4μm, thickness 0.7μm, spacing between lines 0.6μm, distance to the plane 0.6μm. are presented below (fig. 3, fig. 4).

Because of intercepting some flux from the interconnection line by more distant lines Caf and Ccoup of this line decreases. This effect is especially strong for Caf. The more lines are on

both sides of the line, the lower is value of Caf for the middle one. In this case the deviation between the Caf for middle line in 3-lines bus and 15-lines bus is over 13%.

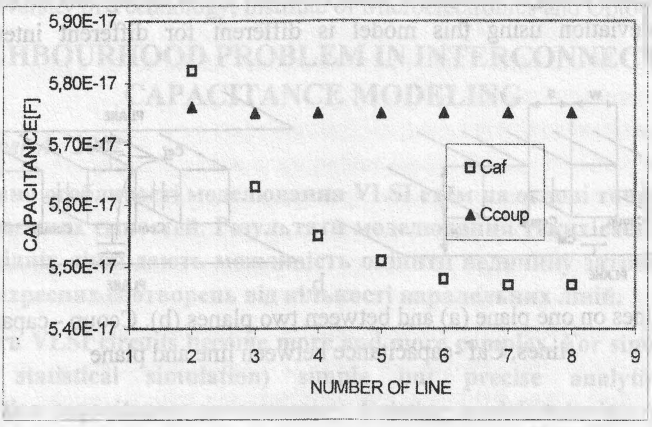

Fig. 3. Capacitances for successive lines in 15-line bus. Lines on one plane

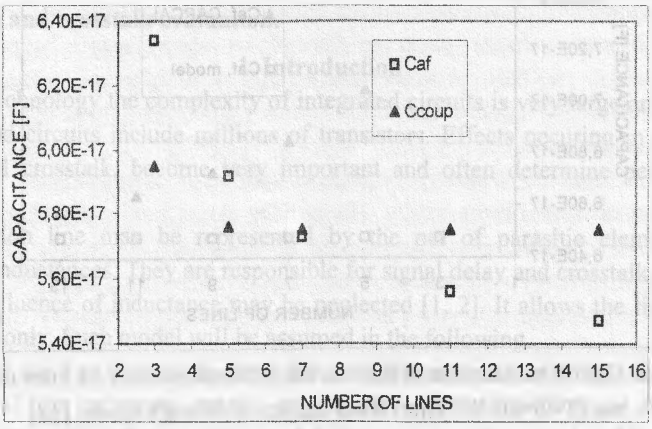

Fig. 4. Capacitances for the middle line for different number of lines in the bus. Lines on one plane.

3. Delay and crosstalk

As it has been shown configuration of further interconnection lines influences values of parasitic capacitances for the modeled one. In order to observe how those differences influence electrical performance of the line, especially delay of the signal in the line and crosstalk, SPICE simulations have been made. The line has been modeled as a net of resistances and capacitances, as shown in fig. 5.

In fig. 6, fig. 7 results of the simulation for lines of dimensions as in previous section are presented. The lines were 10mm long, modeled with 10 resistances, 10 capacitances Caf and 10 capacitances Ccoup to every neighbour. The simulations have been performed for 3-lines model, using values of capacitances taken from numerical extraction for 3-lines bus and 15-lines bus. Presented results show that in this case difference between rising times is over 15% and between crosstalk voltages - over 13%.

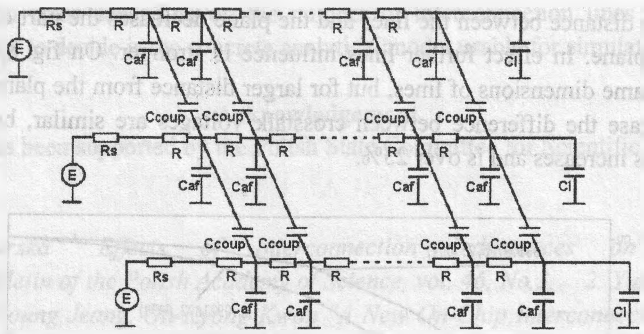

Fig. 5. RC model of three parallel interconnection lines. E - voltage source, Rs - source resistance, Cl - load capacitance

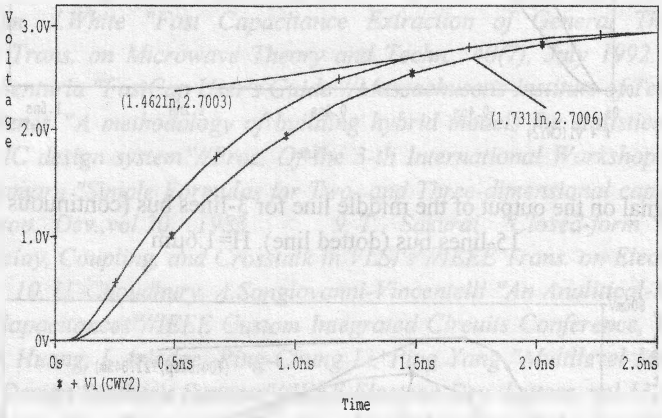

Fig. 6. Signal on the output of the middle line for 3-lines bus (continuous line) and 15-lines bus (dotted line). H=0.6μm

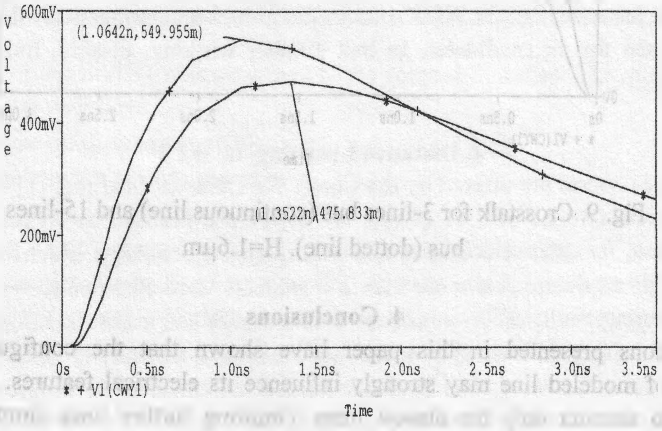

Fig. 7. Crosstalk for 3-lines bus (continuous line) and 15-lines bus (dotted line). H=0.6μm

Increasing the distance between the lines and the plane decreases the part of flux from lines intercepted by the plane. In effect further lines influence is stronger. On fig. 8, fig. 9 results of simulation for the same dimensions of lines, but for larger distance from the plane (H=1,6μm) are presented. In this case the difference between crosstalk voltages are similar, but the difference between rising times increases and is over 23%.

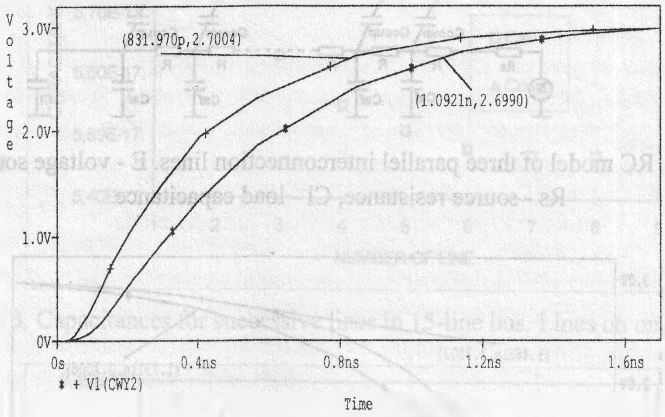

Fig. 8. Signal on the output of the middle line for 3-lines bus (continuous line) and 15-lines bus (dotted line). H=1.6μm

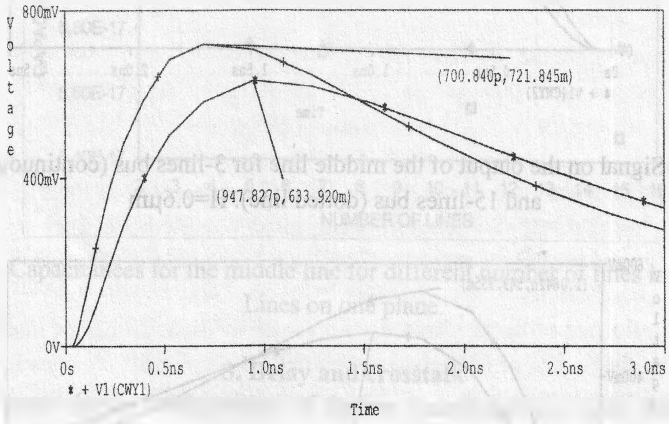

Fig. 9. Crosstalk for 3-lines bus (continuous line) and 15-lines bus (dotted line). H=1.6μm

4. Conclusions

Considerations presented in this paper have shown that the configuration of further neighbourhood of modeled line may strongly influence its electrical features. Simple analytical models take into account only the closest lines. Omitting further lines simplifies capacitance modeling but introduce an error. Numerical analysis has shown significance of the delay time and

crosstalk evaluation error depending on the number of interconnection lines in the bus. Such analysis is necessary to decide is the concrete analytical model usable for simulation purposes.

Acknowledgement

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