4. CONCLUSIONS

When analyzing the measurement results, we can say that the controller with third harmonic limitation circuit, of which operation principles were presented in this paper, operates effectively by limiting the supply network current third harmonic level. The presented controller with third harmonic limitation circuit is maybe a non-conventional solution for the higher harmonic content problem, but its effectiveness combined with simplicity makes it a very interesting solution.

REFERENCES

- 1. http://www.microchip.com/download/lit/pline/picmicro/families/12c67x/30561b.pdf
- 2. http://www.microchip.com/download/appnote/pic18/00857a.pdf

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USING OF MOMENT METHOD FOR PARASITIC PARAMETERS OF PRINTED CIRCUITS IN PLANAR STRUCTURES

Keywords: moment method, parasitic parameters, hybrid circuit

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This paper presents using of moment method for printed circuit residual parameters' calculation in single-layer planar structures. In accordance to the method's assumptions, the relations specifying the potential coefficients for printed circuit with arbitral geometric parameters were determined. Using the Mathcad program, basing on the relations as referred to above, the program was developed for calculation of unitary matrices of parasitic capacities and inductances of printed circuit of mutually parallel lines. In order to verify the developed program operation, the hybrid test printed circuits with different geometric parameters were made. The correctness of calculation procedures within the developed program was experimentally verified using the direct measurement for the capacity and the indirect measurement for the inductance.

1. INTRODUCTION

The planar structures, being the conductive line circuits, placed on a dielectric substrate, are able to collect the electric and magnetic field energy. The measure of this capability is expressed as a value of capacities and inductances of the printed circuit [1, 2]. The lack of analytical relations, specifying the charge distribution within such structure types, facilitates no consistent notation of relations describing the charge value. This problem may be resolved using IT means – one of analytical or numerical methods.

Upon a deep analysis of analytical methods and solutions applied in commercial applications, the moment method was chosen in order to determine printed circuit parasitic parameters. This is an approximate method, derived from weighted residue method. This method,

featuring much more lower processing power consumption, allows to analyze e.g. the magnetic field distributions and their characteristics [3, 4, 5]. In this method, as developed by R.F. Harrington, the analytic equation, describing the space-continuous and time- continuous physical problem, is transformed into the algebraic system of equations.

2. MOMENT METHOD – PARASITIC CAPACITIES OF PRINTED CIRCUIT

In case of hybrid microelectronic circuit structure being analyzed, owing to the lack of information about charge distribution on line surfaces, direct utilization of the relation for determination of the field being induced by such a charge is impossible, and, in turn, for determination of the matrices of parasitic capacities and inductances:

$$\boldsymbol{\varphi}(\mathbf{r}) = \frac{1}{4\pi\varepsilon} \iiint_{V} \frac{\boldsymbol{\sigma}(\mathbf{r}) \cdot dV}{\mathbf{r}}$$
(1)

Proceeding in accordance to the moment method rules and dividing each line into finite, but enough high number of fragments, it may be assumed that the charge within k-th fragment of i-th line has a constant charge density value $\sigma_{i,k} = \alpha_{i,k} \underline{\sigma}_{i,k}$. As presented in Figure 1, $\underline{\sigma}_{i,k}$ describes the unitary value of charge density, but $\alpha_{i,k}$ describes the unknown value of the coefficient determining the value of a charge, accumulated within k-th fragment of i-th line.



Fig.1. The fragment of planar printed circuit with the presentation of the moment method idea and the definition of symbols

When dividing each of M lines into finite number of N fragments, the equation (1) may be also presented in matrix form:

$$\boldsymbol{\phi} = \underline{\mathbf{P}} \cdot \boldsymbol{\alpha} = \begin{bmatrix} \boldsymbol{\phi}_{1} \\ \vdots \\ \boldsymbol{\phi}_{i} \\ \vdots \\ \boldsymbol{\phi}_{M} \end{bmatrix} = \begin{bmatrix} \underline{\mathbf{P}}^{1,1} & \cdots & \underline{\mathbf{P}}^{1,j} & \cdots & \underline{\mathbf{P}}^{1,M} \\ \vdots & \vdots & \ddots & \vdots \\ \underline{\mathbf{P}}^{i,1} & \cdots & \underline{\mathbf{P}}^{i,j} & \cdots & \underline{\mathbf{P}}^{i,M} \\ \vdots & \vdots & \ddots & \vdots \\ \underline{\mathbf{P}}^{M,1} & \cdots & \underline{\mathbf{P}}^{M,j} & \cdots & \underline{\mathbf{P}}^{M,M} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{\alpha}_{1} \\ \vdots \\ \boldsymbol{\alpha}_{i} \\ \vdots \\ \boldsymbol{\alpha}_{M} \end{bmatrix}$$
(2)

In this form of notation, the $\boldsymbol{\varphi}$ and $\boldsymbol{\alpha}$ vectors contain respectively vectors of known φ_i potentials and unknown $\alpha_{i,k}$ charge coefficients, whereas the <u>P</u> matrix is a system of potential coefficient matrices. The rank of the $\boldsymbol{\varphi}_i$ and $\boldsymbol{\alpha}_i$ vectors and the <u>P</u>^{*i*,*j*} matrix is result of the line division level:

$$\boldsymbol{\phi}_{i} = \begin{bmatrix} \boldsymbol{\phi}_{1} \\ \vdots \\ \boldsymbol{\phi}_{k} \\ \vdots \\ \boldsymbol{\phi}_{N} \end{bmatrix} \boldsymbol{P}^{i,j} = \begin{bmatrix} p_{1,1}^{i,j} & \cdots & p_{1,n}^{i,j} & \cdots & p_{1,N}^{i,j} \\ \vdots & \vdots & \ddots & \vdots \\ p_{k,1}^{i,j} & \cdots & p_{k,n}^{i,j} & \cdots & p_{k,N}^{i,j} \\ \vdots & \vdots & \ddots & \vdots \\ p_{N,1}^{i,j} & \cdots & p_{N,n}^{i,j} & \cdots & p_{N,N}^{i,j} \end{bmatrix} \boldsymbol{\alpha}_{i} = \begin{bmatrix} \boldsymbol{\alpha}_{1} \\ \vdots \\ \boldsymbol{\alpha}_{k} \\ \vdots \\ \boldsymbol{\alpha}_{N} \end{bmatrix}$$
(3)

In case of such a problem solution formulation, for each divided line fragment the relation describing the value of charge coefficient must be determined. This corresponds to the potential, which will be produced by the constant charge $\underline{\alpha}_{i,k} \sigma_{i,k}$ in any point within surrounding space. When determining the potential, the (1) equation was directly involved. The problem, related to the dielectric heterogeneity of a planar structure and its influence on the potential value was resolved using the mirror reflection method.

The heterogeneous system was replaced with a p-wire mirror system, with theoretically infinite number of wires. The (4) relation describes the potential value, which the unitary charge, accumulated on, will induce in a central point of n-th fragment of i-th line.

$$p_{k,n}^{i,j} = \varphi\left(x_{k,n}^{i,j}\right) = \frac{(l+m)\sigma_{k}^{i}}{2\pi\epsilon_{0}} \left[\Delta w_{k}^{i} + \left(x_{k,n}^{i,j} - \frac{\Delta w_{k}^{i}}{2}\right) \ln \left|x_{k,n}^{i,j} - \frac{\Delta w_{k}^{i}}{2}\right| - \left(x_{k,n}^{i,j} + \frac{\Delta w_{k}^{i}}{2}\right) \ln \left|x_{k,n}^{i,j} + \frac{\Delta w_{k}^{i}}{2}\right| \right] \\ + \frac{(l-m^{2})\sigma_{k}^{i}}{2\pi\epsilon_{0}} \sum_{p=1}^{\infty} m^{2p-l} \left[0.5 \left(x_{k,n}^{i,j} + \frac{\Delta w_{k}^{i}}{2}\right) \ln \left(\left(x_{k,n}^{i,j} + \frac{\Delta w_{k}^{i}}{2}\right)^{2} + 4p^{2}h^{2} \right) - 0.5 \left(x_{k,n}^{i,j} - \frac{\Delta w_{k}^{i}}{2}\right) \right] \\ \cdot \ln \left(\left(x_{k,n}^{i,j} - \frac{\Delta w_{k}^{i}}{2}\right)^{2} + 4p^{2}h^{2} \right) + 2ph \left(atan \left(\frac{x_{k,n}^{i,j} + \Delta w_{k}^{i}/2}{2ph}\right) - atan \left(\frac{x_{k,n}^{i,j} - \Delta w_{k}^{i}/2}{2ph}\right) \right) - \Delta w_{k}^{i} \right]$$

where $m = (\varepsilon_1 - \varepsilon_2)/(\varepsilon_1 + \varepsilon_2)$, whereas the remaining symbols are defined in Figure 1. Assuming that the **P** matrix is a non-singular matrix, we can calculate its converse, and then the values of coefficients determining the charge density:

$$\alpha = \underline{\mathbf{P}}^{-1} \cdot \boldsymbol{\varphi} = \mathbf{P} \cdot \boldsymbol{\varphi} \tag{5}$$

As the conversed $\underline{\mathbf{P}}$ matrix's measure is capacity, its values may be directly used for calculation of unknown matrix of lines capacity. To achieve the final result, the proper submatrices must be separated in accordance to agreed line division, and each of values must be multiplied by the corresponding line width value. This operation corresponds to the summation of all charges, induced on a given line, accumulated on its dummy fragments, as in the following relation:

$$C_{i,j} = \Delta w_{i,1} \sum_{i=1}^{j} \mathbf{p}^{i,j} + \Delta w_{i,2} \sum_{i=2}^{j} \mathbf{p}^{i,j} + \dots + \Delta w_{i,Ni} \sum_{i=Ni}^{j} \mathbf{p}^{i,j}$$
(6)

The calculation of unitary C_{i,j} capacity in a matrix for M line system is presented in Figure 2.



Fig. 2. The capacity coefficient determination for a printed circuit: a) fragment of a matrix for $C_{i,j}$ *, element b) a capacity matrix for M-line system*

In case of real planar circuits, the potential of each line is determined in relation to the ground line. Considering this and assuming that each circuit creates the electrically neutral structure, the values in capacity matrix for circuit with a reference line must be calculated using the following relation:

$$C'_{i,j} = C_{i,j} - \frac{\sum_{j=1}^{M} C_{i,j} \sum_{i=1}^{M} C_{i,j}}{\sum_{i=1}^{M} \sum_{j=1}^{M} C_{i,j}}$$
(7)

The algorithm for determination of a capacity matrix for three line circuit, in which a third line is a reference line, is presented on Figure 3.



Fig. 3. Example of capacity matrix calculation for three line circuit: a) the procedure, b) the results

The magnetic heterogeneity of all planar structures, produced on laminates or ceramic substrates, allows for direct calculation of inductance matrix for printed circuit, using the following relation:

$$\mathbf{L} = \boldsymbol{\mu}\boldsymbol{\varepsilon} \cdot \mathbf{C}_0^{-1} \tag{8}$$

where C_0 is capacity matrix, as calculated for printed circuit, in which the substrate was replaced with a dielectric surrounding the printed circuit. By the combination of all relations, the program was developed that facilitates calculation of unitary matrices of **C**, **L**, **R**, **G** for mutually parallel line printed circuit with arbitrary geometric parameters.

3. THE EXPRERIMENTAL VERIFICATION OF DEVELOPED PROGRAM

As in accordance to the applied method idea, each line is divided into finite number of elements, and in relations describing the potential coefficients value the summation operator exists, before the calculations are started, the required line division level and number of p_{max} coefficients, corresponding to the number of mirror wires, must be set.



Fig. 4. The effect of mirror wire number p_{max} selection on calculation accuracy for the printed circuit (Figure 6a) with the following parameters: ε_r =9.8, h=0.635, s=0.4-10, w=0.4, N=100

Fig. 5. The effect of line division level N on calculation accuracy for the printed circuit (Figure 6a) with the following parameters: $\Box_r=9.8$, h=0.635, s=0.4-10, w=0.4, pmax=50

The calculations results for printed circuit with mutually variable distance (Fig.4) show that assumption the p_{max} value higher than 20 eliminates the effect of this parameter on the calculations accuracy. The performed calculations for printed circuit with variable width prove such assumption. In case of line division coefficient, in order to achieve a capacity value stability, for line configuration with geometric parameters as in hybrid circuits, it is required to divide a line into about 100 fragments (Fig. 5). Such value is especially critical for a configurations, in which lines are placed very close each other.

To perform experiments, test circuits with mutually parallel lines were made on a alumina substrates (96 % Al_2O_3), with geometric parameters that are characteristic for hybrid circuits (Fig. 6). The selection of alumina 96 % Al_2O_3 substrates is a result of their popularity in most hybrid circuits applications. All test circuits were produced on CeramTek substrates with dimensions of 100×60 mm, thickness of 0.635mm and dielectric constant of 9.8. The were produced using METECH 3511 paste. The capacity and resistance measurements of the conductive lines were performed General Radio automatic RLC bridge model 1683.

<u> </u>		1 \	
a)	20	b)	2.0
	10		1.75
	5.0		1.5
	2.0		1.25
	1.0		1.0
	0.75		0.75
	s = 0.4 mm		w = 0.5 mm

Fig. 6. Example printed circuit topologies: a) the circuit with variable mutual distance and constant width w=0.4mm, b) the circuit with variable line width and constant distance s = 0.4 mm

Good agreement of calculation and measurement results (Fig. 7 and 8), especially for higher capacitances, proves the correctness of calculation procedures developed.



The resonance method was used in order to measure the parasitic printed circuit inductance. To determine resonance frequency of the circuit containing unknown parallel inductance of printed circuit and a reference capacitor, the Advantest R3132 spectrum analyzer, equipped with a tracking generator, was used. The high resistance of test printed circuit, although produced using a low-resistance paste (R_{\Box} = 3m Ω), prevented the bridge balancing during measurements. In case of test circuit with two mutually parallel lines shorted on one end, the inductance measured between remaining terminals equals the sum of each line self-inductances, deducted by self-inductance between them:

$$L_{\rm eff} = L_1 + L_2 - M_{12} - M_{21} \tag{9}$$

The unknown value of the L_{eff} effective inductance was determined basing on the f_r resonance frequency, calculated using the following relation:

Leff =
$$\frac{1 - \omega_{r}^{2} C \cdot L_{C} + \sqrt{(\omega_{r}^{2} C \cdot L_{C} - 1)^{2} - (2\omega_{r} \cdot C \cdot r_{S})^{2}}}{2\omega_{r}^{2} C}; \quad \omega_{r} = 2\pi f_{r}$$
(10)

using the SMD reference capacitor C=100pF (1206 housing). The relation (10) accounts for the effects of the line resistance and the reference capacitor's inductance on the calculated effective inductance.



The calculations results determine the limits, in which the effective inductance may vary for such type of structures. The consistence of calculations and measurements results proves the correctness of inductance calculations using the program developed (Fig.9 and 10).

4. CONCLUSIONS

The developed algorithm and program for calculation of parasitic unitary printed circuit parameters facilitate analyzing factors influencing their values. This program facilitates calculation of unitary printed circuit parameters matrices, necessary to solve the. The telegraph equation's solution facilitates identification of electric signal cross-talks between signal paths via their parasitic parameters. Good consistency of calculation and measurement results for test printed circuit capacity and inductance, proves the correctness of the calculation procedures developed. The calculation procedures, written using the Mathcad software suite, feature full versatility. By changing the function describing the potential coefficient value it is possible, using the same procedures, to calculate the parasitic parameter values for other printed circuit configurations (single-layer with shielding surface, multiplayer, shielded printed circuits). The high calculation speed and non-critical processing power and RAM memory requirements are also program advantages.

REFERENCES

- [1] Wisz B., Sabat W., Kalita W., Sperling D.: Characteristics of Inductive Couplings in Hybrid Microcircuit Structures, 4-nd International Symposium on Microelectronics Technologies and Microsystems, Zwickau, 26-27.10.2000, s. 66-70.
- [2] Kalita W., Wisz B., Sabat W.: Kapazitive Kopplungen in Mehrschichtschaltungen, 5 Zwickauer Automatisierungsforum, Zwickau, 23-24.10.1997, s. 98-101.
- [3] Harrington R.F.: Field computation by Moment Methods, Syracuse University, Syracuse 1968.
- [4] Walker C.S.: Capacitance, Inductance and Crosstalk Analysis, Artech House, Boston 1990.
- [5] Gupta K.C.: Microstrip Lines and Slotlines, Artech House, London 1996.