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SIMULATION OF OUTPUT CURRENT-VOLTAGE CHARACTERISTICS OF MOS TRANSISTORS FORMED ON «SILICON-ON-INSULATOR» STRUCTURES

Keywords: SOI MOSFET, "floating substract", "kink-effect", current-voltage characteristics
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The current-voltage characteristics of SOI MOS-transistors created in thick (0,5 μm) silicon films by recrystallized laser beam is calculated. A equivalent circuit for computation of drain current includes n-MOS-transistor and horizontal npn bipolar transistor, which form simultaneously in technological process. The peculiarity of formed bipolar transistor is that its base isolated by layers of undergate and insulating oxides. For calculation of the current of the bipolar transistor the potential of "floating substract" (the under-channel region in which the holes accumulated under drain voltage), which causes of sharp increasing of drain current in the range of small drain voltage, is obtained. The characteristics obtained have abrupt current drain region, known as "kink-effect", which can be described as summed influence of both transistors and at the same time the avalanche formation of charge carriers caused by ionisation under influence of strong electric field does not play essential role. Experimental current-voltage characteristics satisfactorily describe by the given model.

1. INTRODUCTION

Creation of MOS transistors on the basis of silicon-on-insulator structures is of interest when obtaining basic elements for high speed and radiation-resistant devices in comparison with the devices in bulk single-crystal silicon as well as for building circuits with vertical integration of elements.

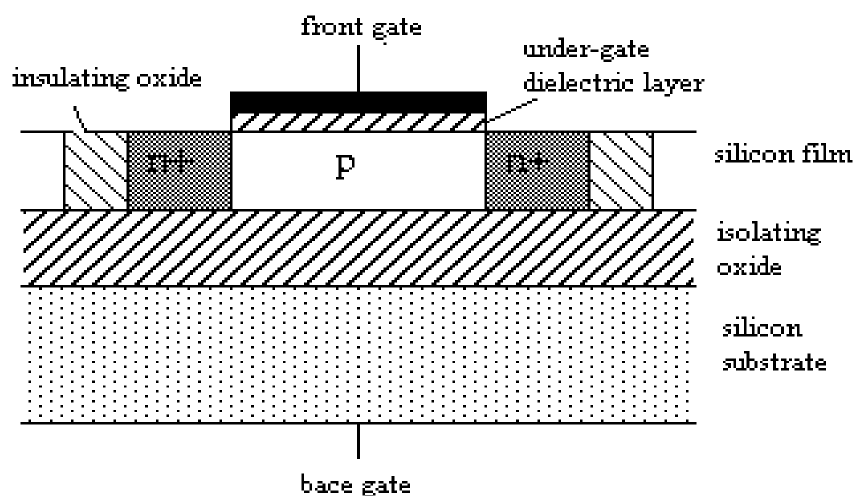

Fig. 1. Schematic drawing of MOS-transistor on the basis of silicon-on insulator structure

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The major component of 3D integrated circuits is a MOS transistor on the basis of silicon-on-insulator structure (fig. 1).

The major difference of the MOS transistor on the basis of silicon-on-insulator structure from the bulk transistor is the presence of a dielectric under the active semiconductor layer that results in the creation of the transistor the current in which can be regulated by two gates simultaneously and the limited thickness of silicon film that is responsible for specific effects in the transistors' operation [1]. Three types of transistors are distinguished depending on the film thickness and doping concentration in the channel: thick-film, thin-film and transistors of medium thickness that work either in thick-film or thin-film modes depending on the bias of the bake gate. In a thick-film silicon-on-insulator device the thickness of the silicon film is double that of the maximum depletion region width x_{dmax} that depends on the concentration of the doping. There is no interaction between the regions of the space charge that stretch from the front to the bake surfaces and there exists a neutral section that causes the emergence of specific effects in the operation of MOS transistors on the basis of silicon-on-insulator, the effect being known as « a kink-effect» and «the effect of drifting substrate» [2]. In a thin-film silicon-on-insulator transistor the thickness of silicon film is less than x_{dmax}. In this case the silicon film is completely depleted at the threshold voltage. The thin-film completely depleted devices actually do not show any kink-effect in case there is no accumulation near the bake surface [3]. Silicon-on-insulator transistors of medium thickness are an intermediate case between thick-film and thin-film transistors. If the bias of the bake gate is such that the front and bake zones of the space charge do not merge then the transistor will behave as a thick-film one. If the bias of the bake gate causes joining of the front and bake depletion zones, then the transistor will behave as a thin-film one. Among all the types of silicon-on-insulator transistors the completely depleted silicon-on-insulator MOS-transistors display the most interesting properties such as high conductivity, low electric fields, a good short-channel mode, quasi-ideal near-threshold bias. However, to form circuits with vertical integration of elements that requires the use of ray technologies to obtain semiconductor films with transistor quality, the silicon layers of 0.5 – 1.0 mkm are used. For this reason, the basic element of 3D integrated circuits is a thick-film silicon-on-insulator MOS-transistor with its inherent specific properties that make it difficult to be used in a traditional form both in analogue and digital integrated circuits.

2. EXPERIMENTAL RESULTS

To estimate the possibility of creating integrated circuits on «silicon-on-insulator» structures in recrystallized layers of silicon with the thickness of 0.5 mkm there were formed p-MOS-transistors with various correlation of geometrical dimensions and their current-voltage characteristics were studied. The typical current-voltage characteristics are presented in fig.2. In the region of the drain current saturation there is observed the effect of the output characteristics kink; the threshold voltage in the transistors under study was being changed from 0.5 to 2.5 V.

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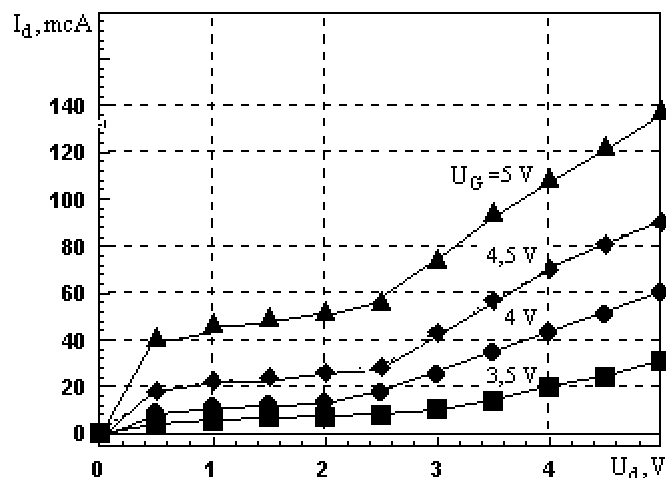

Fig. 2. Experimental current-voltage characteristics of a silicon-on-insulator MOS-transistor

Experimental studies of silicon-on-insulator MOS-transistors (SOI MOS-transistors) functioning have shown that their current-voltage characteristics differ from the characteristics of MOS-transistors created in bulk silicon [4]. A SOI MOS transistor is formed in a thin film of polycrystalline silicon that is isolated from a silicon wafer with a thick layer of a dielectric (fig.1). In a standard technology of semiconductors manufacturing on a structure of this type the contact up to the subchannel region is not ensured. As the silicon film has a large-crystal structure the mobility of charge carriers in it is lower than that in single-crystal silicon. Besides, the layers that lie lower than the silicon film contribute to the redistribution of voltages applied to the transistor electrodes. The maximum depletion regions above and below the poly-silicon layer do not cover the poly-silicon film and there exists a neutral region between the depletion regions that causes the effects of drifting substrate, the kink-effect being one of them. The kink-effect is caused by the injection of holes into the neutral region of a SOI MOS-transistor. It is considered that these holes are generated by ionization of collision near the drain and are accumulated in the region with the lowest potential, i.e. in a drifting substrate. The potential of the neutral region, close to the source junction that is near, can grow in such a way that at the transistor source there will be created a mode of the direct bias for the current from the neutral substrate into the source that will balance the current created by the generation of holes. The growth of the neutral substrate potential causes decrease of the threshold voltage and the kink-effect in the output characteristics of the transistor. The kink-effect is not desirable as it can create current bursts that limit the spheres of transistors application.

3. PHYSICAL CHARACTERISTICS OF SOI MOS-TRANSISTORS

As it has been already shown during the explanation of experimental current-voltage characteristics of SOI MOS-transistors, the kink-effect is caused by the accumulation of holes in the neutral region that causes the creation at the source of the transistor of the direct bias mode for the current from the neutral substrate into the source.

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As it is known, in ordinary MOS-transistors the high-energy hot carriers can cause avalanche creation of pairs of carriers [5]. During this avalanche process there are created holes that are collected by the substrate forming the drifting component of the substrate current. The voltage fall at the substrate resistor caused by this current increases the voltage near the MOS-transistor, in comparison with the voltage of the substrate. For manufacturing MOS IC they usually use substrates with relatively high nominal resistance (~ 5 – 30 Ohm/cm) while the size of transistors themselves can be quite small. For this reason, the voltage fall at the substrate, even when the substrate currents are small, can cause local injection of holes near the drain under the action of avalanche multiplication that can increase the potential of the substrate close to the source junction, situated near, in such a way that the direct bias mode is created at the transistor source. If this local direct bias reaches approximately 0.6V, the injection of electrons from the source to the substrate can start.

The source junction is doped much more than the substrate, so, its coefficient of the electrons injection is very close to 1. As a result, a great number of electrons, in case of direct bias at the source, will get to a narrow region under the channel. Some of these electrons, having been injected by the source, behave in the same way as in a horizontal bipolar npn- transistor and are collected either through the channel region or near the drain. This « bipolar current» itself increases the number of holes that are formed in an avalanche way and return to the substrate as an additional base current for a bipolar npn-transistor.

The mechanisms described can function with rather high multiplication factor so that the holes that are injected into the transistor base can be generated by collector current of a npn-transistor. When this happens, the drain current grows sharply and the breakdown of npn-transistor takes place.

During the formation of a SOI n-MOS-transistor there is simultaneously formed a horizontal npn-transistor with the emitter in the source region, a base which is a low doped under-gate region and a collector at the drain. The peculiarity of the created bipolar transistor is the fact that the bias can not be applied to its base as it is isolated with the layers of under-gate and isolating oxides. When positive voltage is applied to the transistor drain the near-drain region is depleted with the main charge carriers. The holes that are moved from the drain by the sufficient drain voltage are flowing towards the transistor source and are accumulated in the neutral under-channel region, changing its potential. The positive potential in the neutral region, at certain voltages at the drain, is growing to such a degree that there is created the direct bias mode of the emitter-base junction and the bipolar transistor current starts flowing, this current being added to the drain current. Just at this point the current-voltage characteristics of a SOI MOS-transistor show sharp growth of current which is known as the «kink-effect». The equivalent diagram that describes the considered effects is presented in Fig.3.

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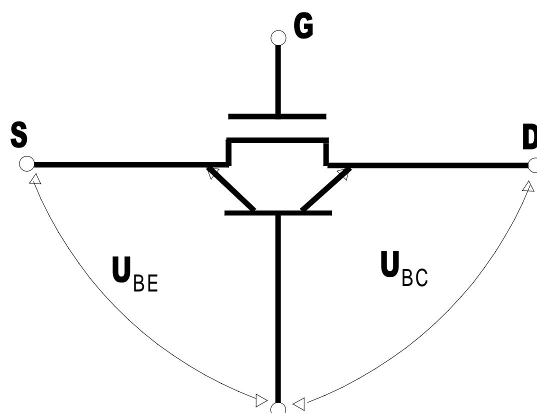

Fig. 3. The equivalent diagram of a SOI MOS-transistor

4. THE MODEL FOR CALCULATING THE OUTPUT CURRENT-VOLTAGE CHARACTERISTICS OF A SOI MOS-TRANSISTOR

According to the proposed equivalent diagram, the summed current of SOI MOS-transistor includes the current of the MOS-transistor itself and the current of the bipolar transistor in which the role of the emitter is played by the source, the base of it is the limited in thickness under-channel region and the collector of which is the drain of a SOI MOS-transistor. With the account of these changes the density of electron current from the first to the second junction can be presented in the following form [5]:

$$J_n = J_s\left[\exp\left(qV_{BC}/kT\right) - \exp\left(qV_{BE}/kT\right)\right], \tag{1}$$

where $J_s = q^2 n_i^2 \tilde{D}_n / Q_B$ is the density of the summed current.

Thus, the summed current is determined in the following way:

$$I_S = \frac{qD_n \cdot n_i^2}{N_a \cdot x_B} \quad . \tag{2}$$

The electron current flowing through the transistor will be:

$$I_n = J_n \cdot A_B, \tag{3}$$

where A_B is the area of the base.

According to the equation (1), under the effect of voltages at the junctions the current I_n can both switch on and switch off. If both voltages V_{BE} and V_{BC} are negative and much larger than kT/q, then the current I_n is negligibly small. If at least one of these voltages is positive and largely exceeds kT/q, then the current I_n will greatly depend on this voltage.

Thus, to calculate the current of a bipolar transistor it is necessary to calculate voltages at emitter and collector junctions. As the transistor base is completely isolated and there is no contact that could initiate the supply of the potential to it, the voltages V_{BE} and V_{BC} as well as the thickness and the area of the base will depend on the voltage being supplied to the collector (to the drain of the parallel MOS-transistor).

To calculate these values let us consider emitter and collector pn-junctions separately.

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In the state of thermodynamic equilibrium the width of the pn-junction x_d depends on the donor and acceptor concentration and is determined in this way:

$$x_d = x_n + x_p = \sqrt{\frac{2\varepsilon_{s0} \cdot \phi_i}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right)}, \qquad (4)$$

where $\phi_i = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^2}\right)$ is an inbuilt potential of pn-junction.

Let us assume that the donor concentrations in the emitter and collector regions are equal in value (the formation of drain-source regions takes place during the same technological process), each of them being $N_d=1\cdot10^{19}$ cm^{-3}, and the concentration of acceptors in the base is $N_a=2\cdot10^{16}$ cm^{-3} . Knowing that the widths of the depletion regions in the regions of p- and n-type are inversely proportional to the concentrations of the corresponding dopes we can find the width of the base depletion region:

$$x_p = \frac{N_d}{N_a + N_d} \cdot x_d \qquad (5)$$

The volume charge in the transistor base both at the emitter and at the collector pn-junction will be equal to:

$$Q_p = -q \cdot N_a \cdot x_p. \qquad (6)$$

When positive (inverted) bias voltage is applied to the transistor collector (drain) the width of the collector junction will increase:

$$x_d(V_D) = \sqrt{\frac{2\varepsilon_{s0}}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right)(\phi_i + V_D)}, \qquad (7)$$

the value of the volume charge in the base near the collector will increase correspondingly:

$$Q_p(V_D) = -q \cdot N_a \cdot \frac{N_d}{N_a + N_d} \cdot x_d(V_D). \qquad (8)$$

When voltage is applied to the collector, holes are pushed away from the collector junction and because of complete isolation of the base they move towards the emitter junction. The charge in the depletion region in the base near the emitter junction changes:

$$Q_{pE}(V_D) = Q_p - Q_p(V_D). \qquad (9)$$

Its width is changing correspondingly:

$$x_{pE}(V_D) = \frac{Q_{pE}(V_D)}{q \cdot N_a}. \qquad (10)$$

Knowing the charge value in the base near the emitter junction (drifting substrate) and its width, we can calculate how the potential V_{FS} of the drifting substrate is changing when voltage is applied to the collector (drain):

$$V_{FS}(V_D) = \frac{\left[x_{pE}(V_D)\right]^2}{\frac{2\varepsilon_{s0}}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} - \phi_i. \qquad (11)$$

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The voltage applied to the transistor collector(drain) will be distributed in the following way:

$$V_{BE}(V_D)=V_{FS}(V_D) \text{ i } V_{BC}(V_D)=-[V_D - V_{FS}(V_D)]. \quad (12)$$

So, the equation for calculation of the current through the bipolar transistor will look like this:

$$I_n(V_D)=I_s\left[\exp\left(qV_{BC}(V_D)/kT\right)-\exp\left(qV_{BE}(V_D)/kT\right)\right]. \quad (13)$$

Redistribution of the charge in the transistor base changes the value of the summed current I_S because the length of the base is changing due to the changes of regions of the space charge near the emitter and collector junctions. The area of the base A_B is also changing when the positive voltage exceeding the threshold value is applied to the gate of a MOS-transistor. The silicon film thickness is a constant value and equals 0.5 mkm. To determine the base thickness it is necessary to subtract the maximum depletion region thickness, having been formed as the result of the MOS-transistor channel emergence, from the silicon film thickness, the maximum depletion region thickness being equal to:

$$d_{\max}=\sqrt{\frac{4\varepsilon_{s0}\cdot|\phi_p|}{q\cdot N_a}}. \quad (14)$$

The summed current of the bipolar transistor and a MOS-transistor is shown in fig. 4.

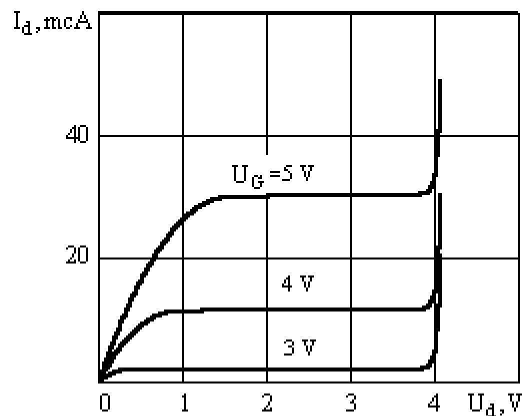

Fig. 4. The output current-voltage characteristics of a SOI MOS-transistor

It is seen in the figure 4 that the drain current of the SOI MOS-transistor is sharply growing when the voltage at the drain is approximately equal to 4V. During the experimental studies of current-voltage characteristics of SOI MOS-transistors the kink-effect was observed at the drain voltages of 2.5 –3V. The calculations are in good conformity with the experimental results at the electrons mobility values of 200 cm^2 /V· s. Discrepancies in the results of theoretical calculations and experimental results are likely to be due to the fact that the calculations done did no make account of physical effects that are int4oduced into the transistor functioning by the presence of the lower gate and the base resistance which can decrease currents flowing through the transistor.

It is interesting to check the calculations done. It is known from literature that when the film is so thin that it is completely depleted during the induction of the channel, there is no kink-effect. While using in calculations of the silicon film the value that is equal to the maximum depletion region width under the channel of MOS-transistor, no sharp growth of current was observed and this is in full conformity with the experimental results known from literature [6].

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5. CONCLUSION

Calculations of the output current-voltage characteristics of SOI MOS-transistors were performed. During the calculations it was assumed that when a MOS-transistor is created according to the standard technology in the thickness-limited silicon film and during the formation of the drain-source regions the depth where high-doped regions are situated automatically reaches the end of the silicon film, then simultaneously a bipolar transistor is formed the functioning of which influences the functioning of a MOS-transistor. The potential of the drifting substrate and the current of the bipolar transistor have been calculated. It has been found that when both transistors are functioning simultaneously in the output current-voltage characteristics there is observed a sharp gain of the drain current known as a kink-effect. The obtained theoretical characteristics are in good conformity with the experimental studies current-voltage characteristics of SOI MOS-transistors.

6. REFERENCES

[1] Colinge J.-P. Silicon-on-Insulator Technology: Materials to VLSI. Kluwer Academic Publishers. 1991, 228 p.

[2] Edwards S.P., Yallup K.J., De Meyer K.M. Two-dimensional numerical analysis of the floating region in SOI MOSFET's. IEEE Trans. Electron Devices. 1988, v.35, p.1012-1019.

[3] Colinge J.P. Reduction of kink effekt in thin-film SOI MOSFET's. IEEE Electron Device Lett. 1988, v.9, p.97-99.

[4] Дружинин А.А., Кеньо Г.В., Когут И.Т., Костур В.Г. Физическая модель КНИ МДП-транзистора для неравновесного состояния. Электронная техника, сер. 3. Микроэлектроника. - 1990.- Вып.5 (139). - С.89-91.

[5] Маллер Р., Кейминс Т. Элементы интегральных схем". М.: Мир. 1989, - 630 с.

[6] Hafes I.M., Chibaudo G., Balestra F. Analysis of the kink-effekt in MOS transistors. IEEE Trans. Electron Devices. 1990, v.37, N 3, Pt.1, p.818-821.

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ABOUT THE NATURE OF THE MAIN PARAMETERS OF TEMPERATURE SENSORS

Key words: kinetic properties, conductivity, dispersion law, scattering

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The results of study of the nature of sensor materials properties are given in this paper. For study of the nature of conductivity and other kinetic properties of semiconductor materials modern kinetic theory was used. The theory is based on statistical sum of large nonequilibrium ensemble of charge carrier gas particles in semiconductors.

Electronic temperature sensors the work of which is based on current passage processes are characterized by several parameters. These parameters depend on kinetic properties of sensor materials. Conductivity is one of these important properties. Study of the nature of conductivity of sensor materials is substantial practical problem of solid-state electronics.

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