5. CONCLUSIONS

A fuel consumption measuring system can reduce costs in a company that uses many vehicles.

Such a system, with high lustiness and reability, low dimension, made with not accesible settings, has a big market in Romania and can be very profitable for the producer and also for its user.

This system is now in testing stage at Hydraulics and Pneumatics Research Institute and we hope it will be produced and sold to customers this year.

6. REFERENCES

[1] G. Ionescu, V. Sgarciu, H. M. Motit, R. Dobrescu, C. Stamate "Transducers for ndustrial automation", Editura Tehnica, 1996, Bucuresti.

[2] MICROCHIP TECHNOLOGY INC., "Embedded control handbook – Volume 1", Microchip Inc., 1997.

[4] M. Ciugudean, V. Tiponut, M.E. Tanase, I. Bogdanov, H. Carstea, A. Filip, "Linear Integrated Circuits", Editura Facla, 1986, Timisoara.

[5] KEITHLEY METRABYTE, "DAS1802ST and DDA08 User's Guide"

[6] Capital Equipment Corporation, "TEST POINT Techniques and Reference", 1996.

[7] SIMTEK, "nvSRAM Data Book", 1999.

Natalija Dorosh, Galyna Kuchmiy

Lviv Polytechnic National University, Department of Electronic Devices
12 Bandery Str., 79013 Lviv, Ukraine.

EFFICIENCY IMPROVEMENT OF MICROELECTRONIC DEVICES FOR SPECTRAL TRANSFORMATION OF SIGNALS

The methods of increase of efficiency of microelectronic devices for spectral transformation of signals are shown, at the expense of use of algorithms of fast spectral transformations with active use of pauses between receipt of readout of a researched signal. The structural organization and functionalities of the digital microprocessor NM6403, on the basis of which it is possible to realize algorithms of spectral transformations in different bases of functions is given .

Introduction. The important direction of development of microelectronics is designing and introduction of the special integrated circuits for realization of algorithms

- spectral transformations in different bases of functions;
- algorithms of a digital filtration;
- algorithms of coding - decoding; modulations and demodulations;
- algorithms for formation (synthesis) of signals of the given form;
- algorithms for organization of the interface and standard protocols of the data transfer.

Such integrated circuits make the conducting world companies as Zilog, Texas Instruments, Motorola, Siemens, Analog Devices.

For realization of spectral transformations frequently use the signals processors (SPU) of the Analog Devices company.

Such SPU work on frequencies F=50-100Mhz, have own codes of commands and are not compatible to processors of other firms. At realization of complex (difficult) algorithms with

parallel structure it is necessary to increase quantity of processors and to provide their joint work in a multiprocessor mode, and also for such processors it is necessary to use external elements of memory. As perspective development now it is possible to consider the processor for digital processing of signals NM 6403, which was designed by technical center "Module" (Russia) [1].

The processor NM 6403 is the high-efficiency special processor with such parameters:
- frequency of the clock generator F=50 Mhz;
- technology CMOS 0.5mkm;
- voltage 2.7-3.6V
- power 1.3 W
- 32 bits RISC structure;
- data processing of variable size from 1 up to 64 bits;
- two 64-bits programming of the interface with external memory;
- two high-speed ports, which is hardware are compatible with signals by the processor $TMS320C4_{x4.}$

The basic subsystems of the processor are RISC - and vector processors. The RISC-processor carries out all basic functions on management of work of the chip and realizes ariphmetic, logical functions and operations of shift above the scalar 32-bit data; forms 32-bit of the address of commands and data at the reference to external memory. The processor is constructed under the circuit 5 - step 32-bit of the conveyor. The size of memory - 16Gб, and also 8 general and 8 address registers. Each commands can be executed for one machine step.

The vector processor is intended for arithmetic and logic operations above 64-digit vectors of the data of programmed word length. The exchange given between the basic units of the processor occurs on three internal trunks, two entrance and one target trunk.

The vector processor - basic functional element NM6403 (Л1879ВМ1). Structurally it represents the matrix-vector operational device and set of the registers of various assignment.The operational device (OD) - regular matrix structure 64x64 of cells.

The matrix can be arbitrary divided into columns and rows. The weight factors W_{ij} are loaded into the cells, formed after division. On an input of a matrix the vector of the entrance data $\vec{X} = (X_1, X_2, \ldots, X_n)$ moves, to which each element there corresponds a line of a matrix. Width of a line (in bits) - word length of the given element of the entrance data. In the cells there is a multiplication of an element of a vector of the entrance data to weight factor and addition to meaning of the top cell (or meanings of inputs U_i). Thus, for each column the scalar product is calculated. $y_i = U_i + \sum_j W_{ij} X_j$

For decrease of word length of the target data and protection against arithmetic overflow the programmed function of saturation is used.

The operands and target meanings are packed into 64 digit words. All operations in a matrix ОУ makes in parallel, for one step. The loading of weight factors occurs for 32 steps. In the vector processor there is a "shadow" matrix, into which the weight factors can be loaded in a background mode. The switching "shadow" and worker of matrixes borrows one step. Major feature of the vector processor - work with operands of any length (even not multiple degree двойки) in a range of 1-64 bits. It reaches an optimum ratio between speed and accuracy of calculations: at one-bit operands on clock frequency 40 Mhz the productivity will make 11 520 MMAC (millions operations of multiplication with accumulation) or 40 000 MOPS (millions logic operations per one second), at 32-bit operands and 64-bit result it becomes .

In a fig. 1 the structural organization of the vector processor is given

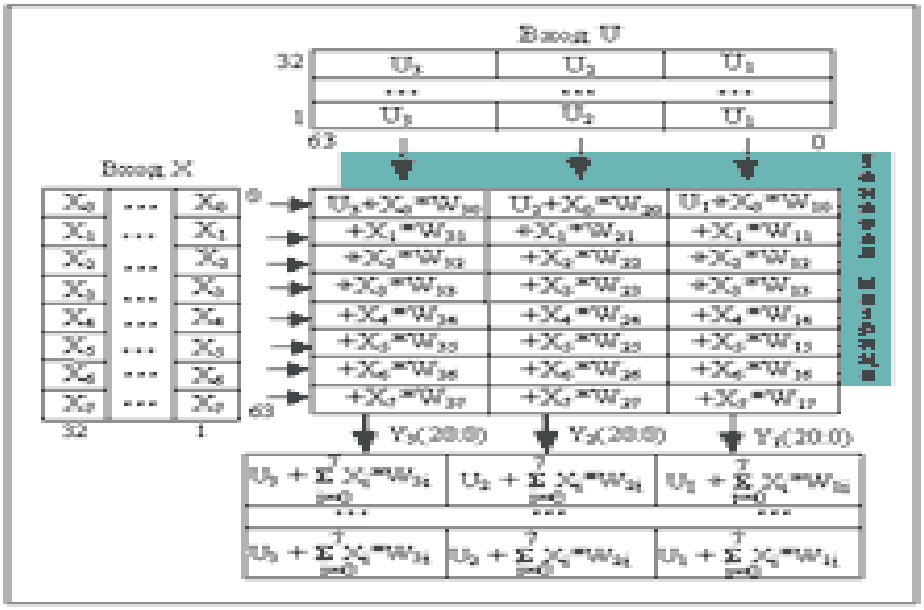

Fig. 1. Structural organization of the vector processor

Technical parameters that to feature of mainframes of the processor is submitted i below:

RISC-NUCLEUS

· 5- the step 32-digit conveyor;
· 32- and 64-digit teams (two operations in one team) are usually carried out;
· two address generators, address space - 16 Гбайт;
· two 64-digit programmed interfaces with SRAM/DRAM-divided memory;
· a format of the data - 32-digit whole;
· the registers:
- 8 32-digit registers of general assignment;
- 8 32-digit address registers;
- special registers of management and condition;
· two high-speed communication ports of an input / conclusion, are hardware compatible with ports TMS320C4x.

VECTOR-PROCESSOR

· variable 1-64-bits length of vector operands and results;
· a format given - integers packed into 64-digit blocks, in the form of words of variable length from 1 up to 64 categories everyone;
· support of векторно-matrix and матрично-matrix operations;
· two types of functions of saturation on a crystal;
· three internal 32x64-digit RAM-blocks.

Productivity:

· scalar operations:
- 40 MIPS;
- 120 MOPS for the 32-digit data;
· vector operations: nominal - 40 MMAC. The skill is dynamical, during calculations to change word length of operands allows to increase productivity.

The microprocessor NM6403 enables realization of discrete spectral transformations in various orthogonal bases by a matrix method. The change of weight factors, which are written

down in cells of the matrix processor, is equivalent to a choice of basis, in which to be carried out the spectral analysis. Besides, if in cells to write down values of weight factors, which correspond to values of a matrix elements of mutual transition between different bases of functions, it is possible easily to count spectral factors in the necessary basis of functions.

The results of testing of the processor NM6403 have shown, that Walsh-Hadamar (WHT) it is possible to execute transformation (21 steps, 5-bit the data) for 0.45 s, and fast Fourier (FFT) transformation (256 points, 32-bit the data) - for 102 mks. The similar tests for processors Intel Pentium 300Mhz: WHT - 2.8 s, FFT - 200mks.

Increase of the spectral analysis efficiency. For increase of efficiency of performance of the spectral analysis in basis rectangular (Walsh) of functions it is necessary to use algorithms fast Walsh transformation [2] .

Amount of operations of addition and subtraction, which are necessary for performance direct Walsh-Hadamar of transformation (matrix method) it is possible to calculate as $L_{WHT}= N*(N-1)$,

Amount of operations of addition and subtraction, which are necessary for performance fast Walsh-Hadamar of transformation (FWHT) it is possible to calculate as

$$L_{FWHT}= N*\log_2 N,$$

where N - dimension of transformation, $n=\log_2 N$ - amount of iterationse .

For increase of speed of devices, which realize FWHT according to standard algorithm of fast transformation, the time between receipts of readout of a researched signal (time of a pause) can actively be used for realization of intermediate calculations. To begin calculations it is possible already after receipt of first two readout of a signal. After arrival of the following two readout it is possible to proceed to the second iteration, and the transition to third iteration is possible after arrival 7 and 8 readout of a signal and so on. The transition to each following iteration is possible after arrival everyone 2^n readout.

Amount of operations, which will be necessary for executing after receipt by last soar of readout at realization of algorithm FWHT with active use of pauses (FWHT-P) it is possible to define as

$$L_{FWHT-P} = 2+2^2+2^3+2^4+...2^n =2(2^n-1)$$

Table 1

$N=2^n$	N=8 n=3	N=16 n=4	N=32 n=5	N=64 n=6	N=128 n=7	N=256 n=8	N=512 n=9	N=1024 n=10
$L_{WHT}= N*(N-1)$	56	240	992	4032	16256	65280	261632	1047552
$L_{FWHT}= N*\log_2 N$	24	64	160	384	896	2048	4608	10240
$L_{FWHT-P}=2(2^n-1)= 2+2^2+2^3+2^4+...2^n$	14	30	62	126	254	510	1022	2046
$K1=L_{WHT}/L_{FWHT}$	2.3	3.75	6.2	10.5	18.1	31.8	56.7	102.3
$K2=L_{FWHT}/L_{FWHT-P}$	1.7	2.1	2.58	3.05	3.52	4.02	4.5	5.0

In a Table 1 dependence of amount of computing operations L (K1, K2) from dimension of transformation N are given.

Conclusion. On the basis of the carried out(spent) analysis of efficiency of algorithms of spectral transformations in various bases is established, that the algorithm of fast transformation with active use of pauses in basis of rectangular functions Уолша allows to define(determine) spectral structure of a researched signal most quickly. The application of such algorithm is expedient at the analysis of signals of low frequency, when the time between receipt of readout of a researched signal has enough for realization of necessary calculations.

The algorithms of spectral transformations can be realized on the basis of digital processor NM6403. The choice of required basis of functions can be carried out by replacement of weight factors, which can be written down in cells of the vector processor NM6403.

[1] http://www.module.ru/
[2] N.Dorosh, G.Kuchmij, Modelling of SCPU-Blocks of Microprocessor Systems // Proceedings 2-nd International Symposium on Microelektronics Technologies and Microsystems. Lviv, 1998, pp.171-174.

УДК 621.317

Oksana Bojko[1], Oleksandra Hotra[2], Petro Stolyarchuk[1]

[1]Lviv Polytechnic National University, Department of metrology, standardization and certification, 12 Bandery Str., 79013 Lviv, Ukraine.
[2]Lviv State Medical University, Department of biophysics, 69 Pekarska Str., 79010 Lviv, Ukraine.

STRUCTURE METHODS OF COMPENSATION OF COMMUNICATION LINES INFLUENCE BY CURRENT IN ACTIVE RESISTANCE SIMULATORS

Key words: four-wire active resistance simulator, compensation of communication lines influence

The structure methods of compensation of communication lines influence by current in four-wire active resistance simulators with transmission functions $R_{sim}=R_0\mu$, $R_{sim}=R_0(1-\mu)$ are considered.

Active simulators are widely used because of their advantages over classic resistance boxes [1-3]. The main advantage of active resistance simulators is the possibility of resistance reproduction with necessary accuracy in the points, which are placed on big distances from device.

Different transmission functions are used at designing of active simulators [4,5]. But the most spread functions are the following [6,7]

$$R_{sim}=R_0\mu, \quad R_{sim}=R_0(1-\mu),$$

where R_{sim} is the value of simulated resistance, R_0 is the standard resistor resistance, μ is the gain of code-controlled voltage divider (CVD).

To provide necessary accuracy at resistance simulation on big distances it is necessary to decrease the influence of communication lines resistance. There are two types of compensation circuits of communication lines influence: compensation circuits by voltage and compensation circuits by current. The compensation by voltage consists in separation of voltage drop on communication line and in subtracting of it from output voltage of input amplifier. Compensation by current consists in formation of compensating current I_c which is proportional to voltage drop on the communication line resistance, i.e. $I_c=f(I_{in},R_L)$, where I_{in} is input current, R_L is the resistance of communication line.

Generalized structural diagrams of active simulators of resistance with compensation of communication lines influence by current are given in Fig.1.

Four-wire connection circuit compensates the communication lines influence of output operational amplifier and the influence of the line connected with the input of the first amplifier.