The Fig. 7 shows that for the same compression ratio, wavelet decomposition has less relative error or, for the same error, it can achieve a larger compression ratio.

CONCLUSONS

A problem of choosing the proper compression method for signals obtained from fibre-optic flame monitoring system was presented. Such signals are highly nonstationary, where sudden changes of amplitude take place. Wavelet based compression gives better results comparing to Fourier transform based compression for such signals. The same amount of signal's energy is contained within smaller number of expansion coefficients for the wavelet transform. Moreover, relative errors for the same compression ratios are smaller using the wavelet transform.

A care must be taken choosing the proper wavelet basis [4] in order to achieve as small relative errors as possible.

Wavelet based compression can be applied in real-time with modern DSP processors, the more, so as wavelet transform computed especially, that in the case of Daubechies wavelets, consumes less time than FFT algorithm does.

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THE REFLECTIONS PRODUCED BY LUMPED LOAD OF DIGITAL SIGNAL LINE

Key words: printed circuit board, reflections, digital circuits, capacitance load.

In interconnection technique of digital circuits in general the matched lines method for reducing the influence of reflections in a view to a good working of interconnected circuits is used. Due to the input capacitance of digital circuits appears a reactance load. Although the matching is very good realized from the viewpoint of the resistive load, there is a reactive mismatching that can produce reflections at high frequency. Using Laplace transformation the reflections produced by parasitic capacitance load will be determined. These reflections will be analyzed depending on the type of the digital circuits and the parameters of the interconnection line. For some types of digital circuits the maximum fanout from this point of view will be determined.

1. INTRODUCTION

In digital systems the designer has to take care of line reflections caused by improperly terminated lines. These line reflections may lead to additional signal distortion which cause

incorrect detection of the value of the signal at the line end (receiver input). This may result in a false operation of the system and increase the electromagnetic emission.

Reflection phenomenon is well known from the transmission line theory [1-2]. The voltage of the reflected wave depends on: the output impedance, the voltage swing and the transition time of the transceiver circuit, input impedance of the receiver circuit, characteristic impedance and propagation time of the interconnection line [3-7]. The influence of the reflected voltage to a good function of the receiver circuit depends on the noise immunity of this circuit.

In interconnection technique of digital circuits, for reducing the influence of reflections in view to a good working of interconnected circuits, two methods are generally used: reducing the length of the signal line under the maximum length and the matching line [3-9].

2. THE REFLECTIONS DUE TO THE CAPACITIVE LOAD

The matching of signal line may be realized at input of the line, by placing a resistor between the output of the transceiver circuit and input of line and at the output of the signal line, when, in function of the type of digital circuit, the number of receiver digital circuits, the placement of receivers digital circuits (to along or the end of the signal line) one of methods which are presented in figure 1 may be used.

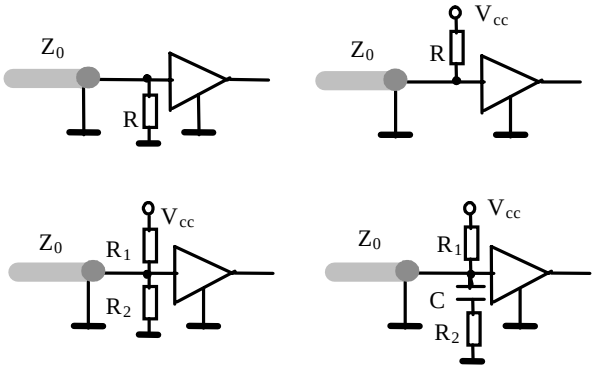

Fig. 1. Some methods for matching at output line

In generally the inductance of the matching circuit is smaller, but the capacitance load may become bigger. There are two ways of placing digital circuits on a parallel terminated transmission line: one is called distributed loading, the other lumped load. For lumped load at the end of the digital signal line, the capacitance load increase with the number of the receiver digital circuits, figure 2. Having in view the input capacitance of the digital circuits results the equivalent circuit from figure 3 for applied one of methods for matching of the line at the end.

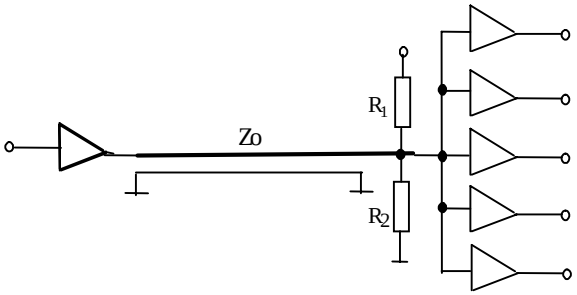

Fig. 2. Lumped load at the end of the line

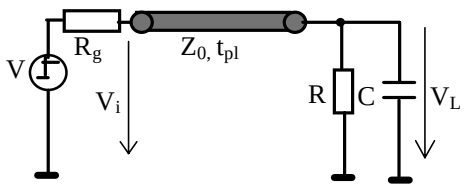

Fig. 3. The equivalent circuit for the matching output line having in view the parasitic capacitance of the digital inputs

The capacitance C is equal to nC_i; n is the number of receveir circuit and C_i is the input capacitance of digital circuit.

The voltage at the input line will be represented as, $V_i(t) = mtU(t) - m(t-t_r)U(t-t_r)$ (1)

where: U(t) is a step function occurring at t =0; m is the slope of the input voltage,

$$m = \frac{(V_{OH} - V_{OL})Z_0}{(Z_0 + R_g)t_r} = \frac{V_s}{t_r} \tag{2}$$

V_{OL},V_{OH}, is the output voltage of digital circuit for L logical state , respectively H; V_S is the voltage swing; t_r is the minimum between the rise and fall time of the digital signal.

Taking the Laplace transformation of equation (1), results:

$$V_i(s) = \frac{m}{s^2}\left(1 - e^{-trs}\right) \tag{3}$$

In this case, the reflection coefficient at the load is:

$$\rho_L(s) = \frac{(R - Z_0) - sRCZ_0}{(R + Z_0) + sRCZ_0} \tag{4}$$

The first reflected voltage at the load, in Laplace notation, is [5]:

$$V_{r1L}(s) = \frac{-\left(s + \dfrac{Z_0 - R}{RCZ_0}\right)}{s^2\left(s + \dfrac{Z_0 + R}{RCZ_0}\right)} m\left(1 - e^{-st_r}\right) \tag{5}$$

Taking the inverse Laplace transformation, results for $R=Z_0$:

$$V_{r1L}(t) = \frac{-V_s CZ_0}{2t_r}\left[\left(1 - e^{-\frac{2t}{CZ_0}}\right)U(t) - \left(1 - e^{-\frac{2(t-t_r)}{CZ_0}}\right)U(t-t_r)\right] \tag{6}$$

Denoting with:

$\tau_C = Z_0C$, the time constant and $\tau = \tau_C/t_r = Z_0C/t_r$, equation (6) become,

$$V_{r1L}(t) = \frac{-V_s\tau}{2}\left[\left(1 - e^{-\frac{2t}{\tau_C}}\right)U(t) - \left(1 - e^{-\frac{2(t-t_r}{\tau_C}}\right)U(t-t_r)\right] \tag{7}$$

The maximum reflection voltage is for $t=t_r$ and from equation (6), respectively (7) results,

$$V_{r1L\max} = -\frac{V_s CZ_0}{2t_r}\left(1 - e^{-\frac{2t_r}{CZ_0}}\right); V_{r1L\max} = -\frac{V_s\tau_C}{2t_r}\left(1 - e^{-\frac{2t_r}{\tau_C}}\right); V_{r1L\max} = -\frac{V_s\tau}{2}\left(1 - e^{-\frac{2}{\tau}}\right) \tag{8}$$

Figure 4 presents the voltage for the first reflection. In figures 5-7 PSpice simulations results for different values of capacitance load C, characteristic impedance of the line Z_0 and the rise time of digital signal t_r are shows, respectively.

From equations (6)-(8) and figures 4-7 results some generally conclusions: the voltage of the reflections produced by parasitically capacitance is direct proportional with the voltage swing and input capacitance of the digital circuit, with the characteristic impedance of the interconnection line; the voltage of the reflections is inverse proportional with the rise time of the digital signal; the voltage of the reflections is direct proportional with the time constant τ_C and the ratio $\tau=\tau_C/t_r$.

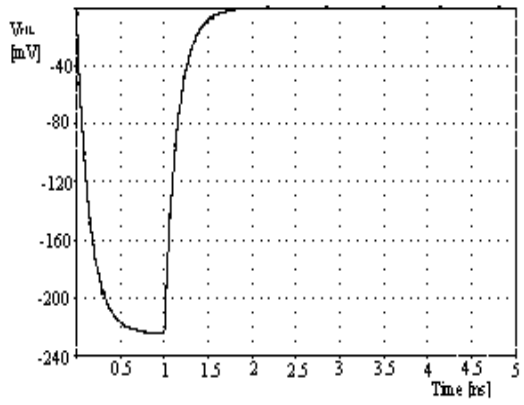

Fig. 4. The voltage of the first reflection at the load for V_s=3V, Z_0=R=50Ω, t_r=1ns, t_{pl}=0.5ns, C=10pF

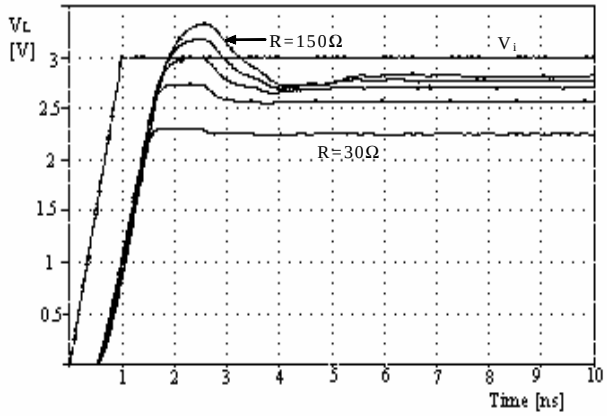

Fig. 6. The load voltage V_L for V_s=3V, t_r=1ns, t_{pl}=0.5ns, C=3 pF, Z_0=R={30; 60; 90; 120; 150}Ω

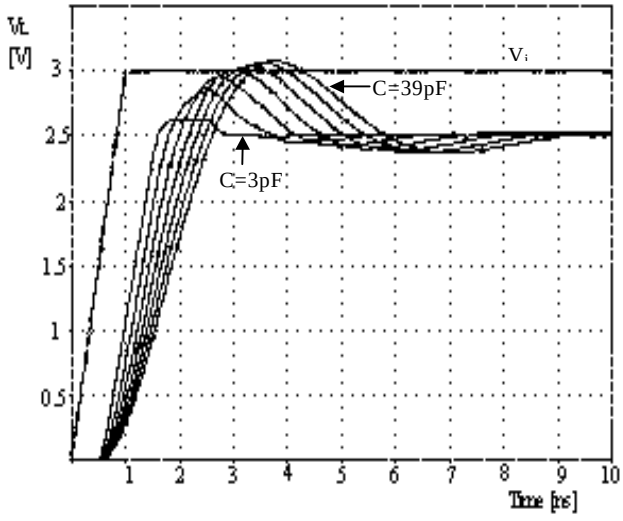

Fig. 5. The load voltage V_L for V_s=3V, t_r=1ns, Z_0=R=50Ω, t_{pl}=0.5ns,C={3; 9; 15; 21; 27; 33; 39}pF

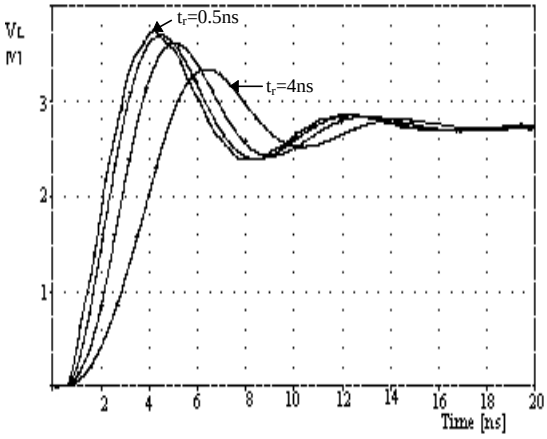

Fig. 7. The load voltage V_L for V_s=3V, t_{pl}=0.5ns, C=30pF, Z_0=R=100 Ω, t_r={0.5; 1; 2; 4}ns

3. ANALYSIS OF THE REFLECTIONS DUE TO LOAD CAPACITANCE IN FUNCTION OF THE TYPE OF DIGITAL CIRCUIT

For a generally characterization of the reflections produced by the load capacitance in function of the type of the digital circuit, it is necessary to know: the voltage swing, the noise immunity and the input capacitance of the digital circuit, the rise and the fall time of the digital signal, which are approximately equal with the transition time of the digital circuit.

Table 1 presents the typical voltage swing V, the typical input capacitance $C_{i,}$ the typical rise time t_r, the voltage of guaranteed noise immunity V_{NI} for some types of the digital circuits and the voltage of guaranteed noise immunity V'_{NI}, having in view the simultaneously action of all types of perturbations (reflections, crosstalk, impedance coupling of the power supply line, electric, magnetic and electromagnetic reception) [9-11].

Table 1

The voltage swing V, the input capacitance C_i, the rise time t_r and the guaranteed noise immunity V_{NI} and V'_{NI} for some digital circuits.

Digital circuit	LV	LVC	LVT	ALVC	ECL 10K	ECL 10KH	CMOS	HC	AHC	AC	HCT	AHCT
V [V]	3	3	3	3	0.8	0.8	5	5	5	5	3	3
C_i [pF]	2.5	5	4	6	3.3	2.9	5	3	3	4	3	3
t_r [ns]	6	3.7	3	2.5	2.5	1.8	60	5.5	6.2	2.7	3.3	3.7
V_{NI} [mV]	o.4	0.4	0.4	0.4	0.1	0.1	1.4	1.4	1.4	1.4	0.4	0.4
V'_{NI} [mV]	0.1	0.1	0.1	0.1	0.025	0.025	0.35	0.35	0.35	0.35	0.1	0.1

The value of parameters C, Z_0, t_r for different practical case may be considerate: C=3…40 pF; Z_0=20…150 Ω; t_r=0.5…10 ns. Result: τ_C=20ps…6ns.

Have in view the expression (8), results:

- if τ<1/6, respectively $(Z_0C)/t_r$<1/6, the maximum of the first reflection is,

$$V_{r1Lmax} = (-V_s\tau)/2 \tag{9}$$

- if τ>1/2, respectively $(Z_0C)/t_r$>1/2, the maximum of the first reflection is,

$$V_{r1Lmax} = (-V_s)/2 \tag{10}$$

The first condition for reduce the reflection due to capacitance load is,

$$\frac{Z_0 n C_i}{t_r} \le \frac{1}{6}, \text{ and results the fanout, } n \le \frac{t_r}{6Z_0C_i} \tag{11}$$

Another solution to reduce the influence of reflection due to capacitance load for the good function of the digital circuits is to reduce the voltage of this reflection under the voltage of noise immunity. Having in view that the maximum voltage of reflection is the voltage of the first reflection, results the condition:

$$V_{r1L\max} \le V_{NI} \tag{12}$$

From expressions (9) and (12) results the maximum time constants τ_{CM}, respectively τ'_{CM},

$$\tau_{CM} = \frac{2V_{NI}t_r}{V_s} \tag{13}$$

$$\tau_{CM}^{©} = \frac{2V_{NI}^{©} t_r}{V_s} \tag{14}$$

The maximum fanout n_M, respectively n'_M, will be:

$$n_M = \frac{2V_{NI} t_r}{V_s Z_0 C_i} \tag{15}$$

$$n_M^{©} = \frac{2V_{NI}^{©} t_r}{V_s Z_0 C_i} \tag{16}$$

In table 2, the maximum time constants for different type of digital circuits are presented.

Table 2

The maximum value of time constants τ_{CM}, τ'_{CM} for different digital circuits

Digital circuit	LV	LVC	LVT	ALVC	ECL 10K	ECL 10KH	CMOS	HC	AHC	AC	HCT	AHCT
τ_{CM} [ns]	1.6	1	0.8	0.66	0.62	0.36	33	3	3.4	2.5	0.88	1
τ'_{CM} [ns]	0.4	0.25	0.2	0.16	0.15	0.09	8.4	0.7	0.8	0.37	0.22	0.24

Having in view the computed dates which are presented in table 2, some general conclusions results: for CMOS, HC, AHC, AC and LV circuits the reflections due to capacitance load have a small amplitude of the voltage, under the voltage of noise immunity, for practical case; for HCT, AHCT, LVT, LVC, ALVC circuits it is possible than the amplitude of reflection voltage to be bigger than the voltage of noise immunity and will be necessary to reduce the fanout; for ECL circuits it is necessary to reduce at minimum the parasitic inductance and using a small fanout.

Knowing the type of the digital circuit (transition time, input capacitance), the type of the signal line (characteristic impedance), results the maximum fanout. For example: for a line which have a characteristic impedance equal with 50 Ω and AC digital circuits, results approximately seven for the maximum fanout.

4. CONCLUSIONS

When a matching circuit is used at the end of the line, a reactance load appears due to parasitic inductance of the matching circuit components and input capacitance of the digital circuit. Although the matching is good realized from the viewpoint of the resistive load, this reactance load produce reflections witch can influence the good function of the digital circuit and increase the electromagnetic emission.

The voltage of the reflections produced by the capacitance load is direct proportional with the input capacitance, the voltage swing of the digital circuit, the fanout and characteristic impedance of the signal line; it is inverse proportionally with the rise or fall time of the digital signal; it is direct proportionally with the time constant. A global parameter for characterize the reflection due to capacitance load is the ratio of the time constant and the transition time of the digital circuit; this parameter is necessary to be smaller in order to results small reflections.

For low and medium speed digital circuits (CMOS, HC, AHC, AC, LV, LVC, TTL, LS) this reflections have a small amplitude of the voltage and may be generally negligible. For high speed digital circuits (ECL, HCT, AHCT, LVT, ALVT, AS) the voltage of the reflections may be up to

the voltage of noise immunity and may influence the good function of the circuits. For this circuits it is necessary to reduce at minimum the parasitic inductance, using the high frequency components (resistors and capacitors) for the matched circuit and using a small fanout for reducing the equivalent capacitance load.

The maximum fanout is direct proportionally with the noise immunity voltage and the transition time of digital circuit; it is inverse proportionally with the switching voltage and input capacitance of digital circuit and the characteristic impedance of the signal line.

Have in view the type of digital circuit (transition time, noise immunity, switching voltage, input capacitance), the type of interconnection line (characteristic impedance) the designer may approximate the fanout in order to obtain reduced reflections.

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