Form values of friction coefficient which has been measured is evident that:
- Friction coefficient depends on Centre Line Average value of surface (R_a) of inclinated plane´s surface. However ratio f_{s1}/f_{s2} is with every single surface remarkable.

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ON-LINE SUBTRACTION METHOD FOR MAINS INTERFERENCE REMOVING FROM ECG SIGNALS WITH SIGNAL PROCESSOR

Keywords: ECG signal, on-line, notch filter, subtraction method, DSP

In this article we described the subtraction method for removing mains interference from ECG signals and realized its algorithm in real time by digital signal processor. Tree filtering procedures included in our algorithm are organized as separate modules, which permit us to apply various types of filters without changing the main structure of the algorithm. This organization is very useful and gives us a possibility to analysis and optimization of the subtraction method.

1. INTRODUCTION

There are many methods for suppressing mains interference from electrocardiosignals (ECS). Analog and conventional digital filters are not effective, because they affect some of the useful high frequency signal components adjacent to the mains frequency. This is due to the fact that frequency spectrum of most biomedical signals superimposed with those of mains interference

(50/60 Hz). Therefor the wave shape of the ECS will be distorted after passing a filter, especially in high frequency area as QRS complexes.

All this inconveniences is effectively avoided by applying simple digital filtering only in linear segments of the signal, where there are no significant electrocardiogram (ECG) components. In nonlinear segments the true values are found by subtracting the interference values computed from the nearest linear segment. This subtraction method totally eliminates power-line interference and preserves all original signal components. The inventors of this method have been using this procedure since 1980 and have been implemented it in a family of microcomputer based standard ECG machines. No distortions of the signal have been detected during these years that the procedure has been used. Subtraction method does not affect the signal shape and is comparatively fast. It can be used for simple and fast on-line rejection of mains interference [1], [3]. In order to speed up the subtraction procedure we intend to use a digital signal processor (DSP) [4]. By means of integrated development environment for DSP we simulate the subtraction method in real time.

2. ANALYSIS OF THE SUBTRACTION METHOD

Block diagram of the subtraction method for digital rejection of mains interference [2] is shown on Fig. 1.

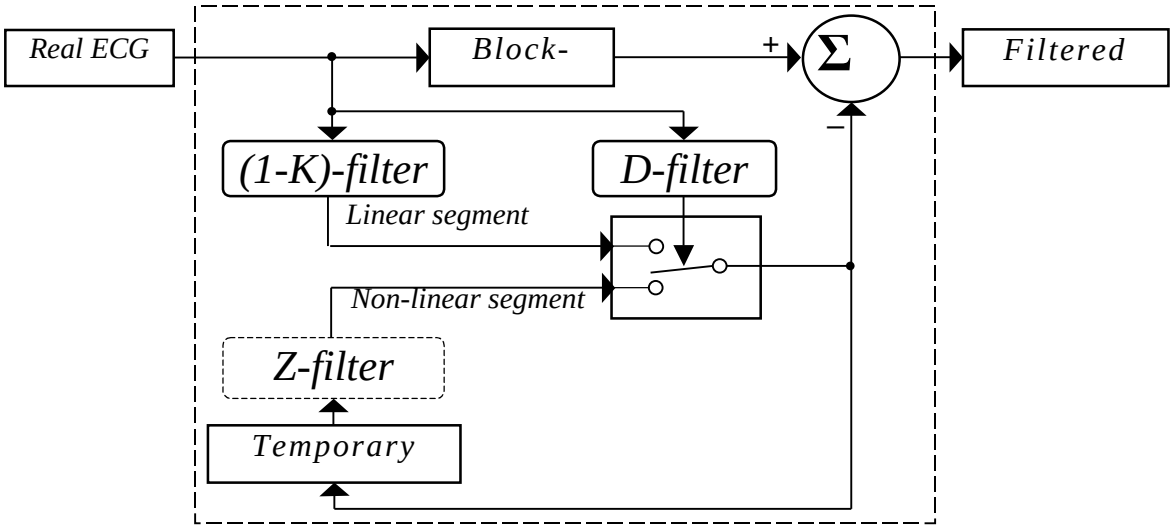

Fig. 1. Block diagram of the subtraction method

The block diagram contains several sub-blocks described as follows:

1) The samples from the input ECS pass through a digital procedure, named D-filter;

2) Every sample of the input signal is checked up whether it belongs to a linear segment of the real ECS. This is done by the switch position (linear or non-linear segment), depending on the result from inequality $A|D| \le M$, named criteria for linearity. There A is a maximal resolution of the input analog to digital converter (ADC), M determines the maximal permitted error and D is the returned value from D-filter;

3) By digital filtering procedure, named (1-K)-filter, the interference values in linear segments are extracted and kept into a temporary buffer;

4) Temporary buffer is used to save the samples of the mains interference in linear segments, because these buffered values are used to compensate the interference, where non-linear segments are encountered;

5) A special digital procedure, named Z-filter, is optional and is used to compensate the phase difference between samples in cases, when mains and sampling frequencies are non multiple.

6) Block-delay is used to compensate the delay, which arises from the used D-filter and (1-K)-filter and depends on their type;

7) At the end of the main subtraction procedure the returned values from (1-K)-filter or Z-filter are subtracted from the output values of block-delay to obtain the output values of the filtered ECS;

3. IMPLEMENTATION

In our realization we have used an ADC resolution of 8 bits (*256* levels), i.e. $A=128$, a sampling rate $\Phi=250$ Hz and empirically chosen threshold $M=8$. If the interference frequency F is *50* Hz, the coefficient of multiplication between Φ and F is $N=2n+1=5$, where n is an integer $n=Int[\Phi/2F]=2$.

The implemented algorithm of the subtraction method is represented on Fig. 2.

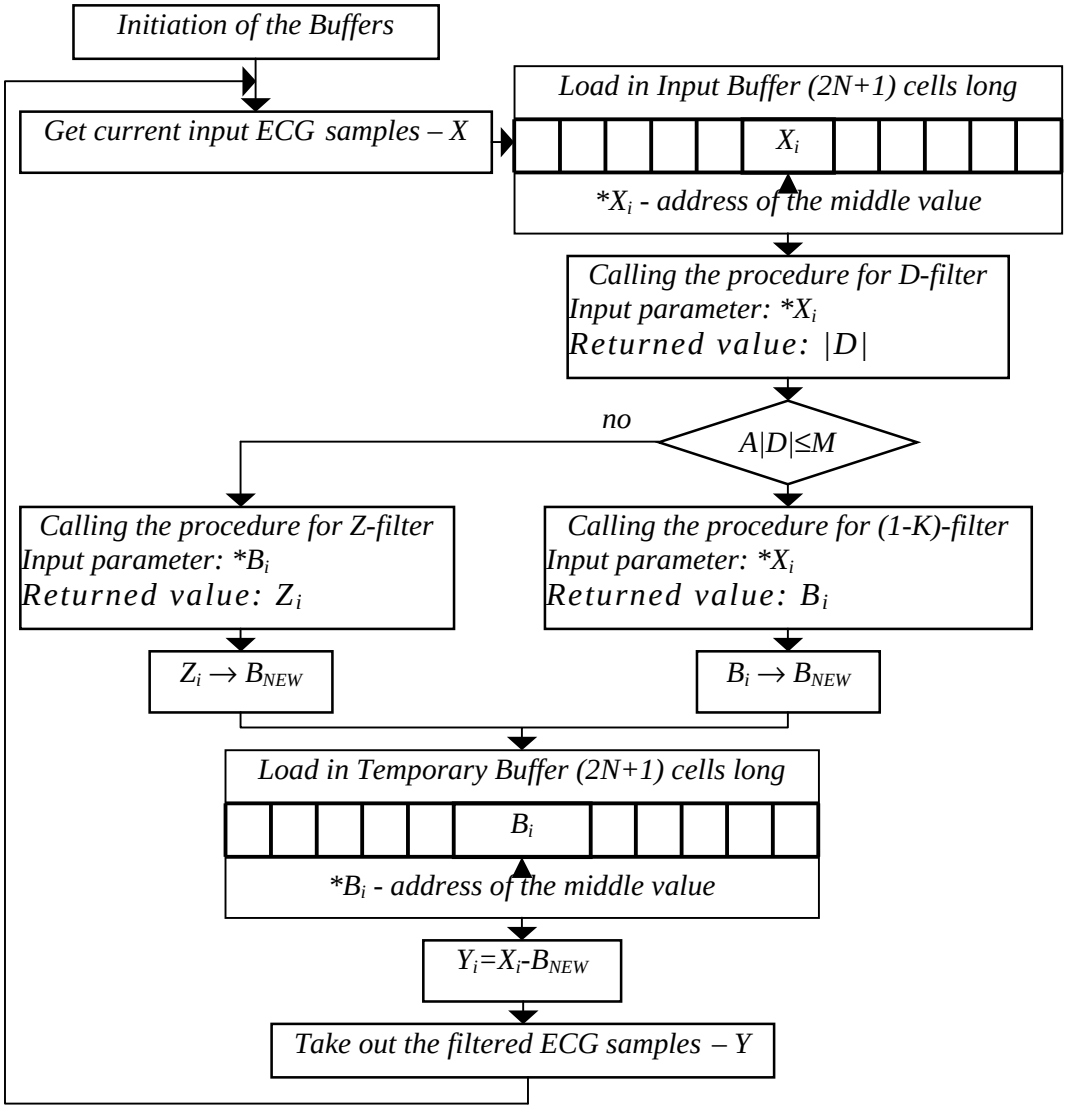

Fig. 2. Algorithm of the subtraction method

1.1. Criteria for estimation of linearity in the ECS epochs – D-filter

First part of the proposed algorithm searches for a linear segment of ECS, according to criteria $A|D|\leq M$, where D is the result from D-filter.

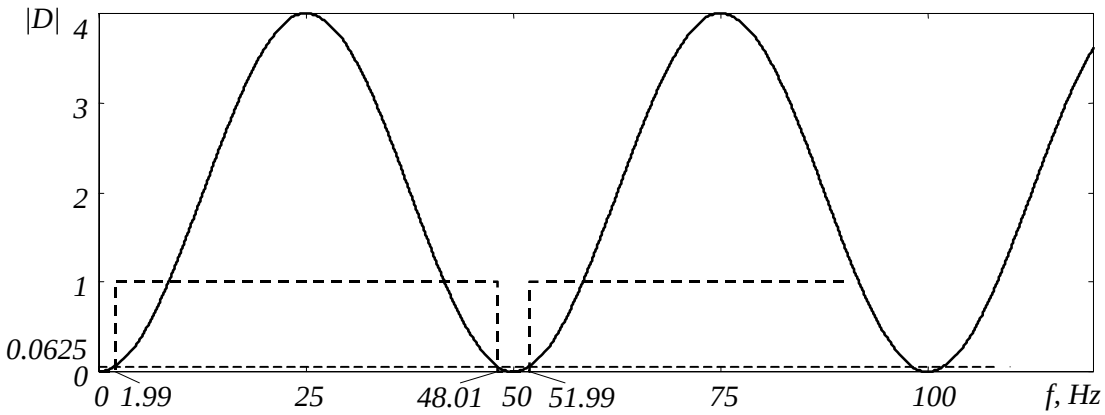

Fig. 3. Transfer response of D-filter defined by difference in Eq. (1)

So far for D-filter has been used the appropriate difference between samples included in one or more periods of mains signal. In our realization for D-filter we have used difference represented by Eq. (1) with transfer response, shown in Fig. 3.

$$D = D_{i+N} - D_i = \left(X_{i+N} - X_i\right) - \left(X_i - X_{i-N}\right) \tag{1}$$

This D-filter defines as linear ECG segments with frequency components from 0 to 1.99 Hz and from 48.01 Hz to 51.99 Hz.

D-filter produced the delay, depending on its type. In our case the delay is one period of mains interference. Block-delay in Fig. 1 is implemented by corresponding length of the input buffer in Fig. 2 and is used to compensate this delay.

1.2. Extracting the mains interference from linear segments – (1-K)-filter

First we used simple moving average FIR K-filter to remove the interference in the linear segments and than we applied (1-K)-filter to extract the mains interference and keep its samples B_i in the temporary buffer.

For our experiments we have used the basal K-filter with Eq. (2), when the sampling frequency is odd-multiple and synchronized to the mains frequency.

$$Y_i = \frac{1}{2n+1} \sum_{j=-n}^{n} X_{i+j}\,, \tag{2}$$

where X_i are original samples, Y_i are filtered samples. The transfer response of the basal moving average K-filter is shown on Fig. 4.

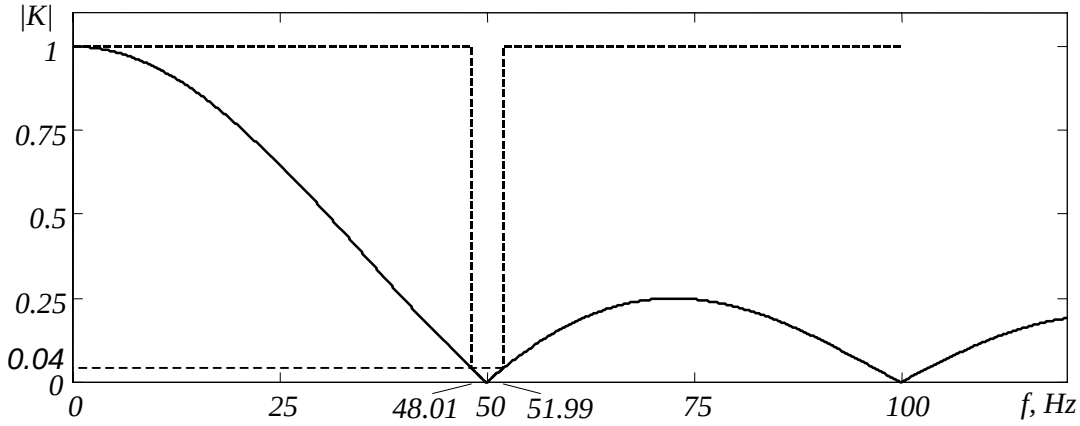

Fig. 4. Transfer response of basal simple moving average K-filter with Eq. (2)

1.3. Subtracting the mains interference from non-linear segments – correction by Z-filter.

The samples of the interference signal from linear segments are used to compose a current interference value, which is subtracted from corresponding value of the input ECS. The interference samples are also kept into a temporary FIFO buffer and are updated continuously. They are used when a non-linear segment is found.

In non-multiple cases there is phase difference between corresponding sample of the mains interference from temporary buffer and the current ECS sample in the non-linear segments. The procedure for compensation of this phase difference is performed by Z-filter.So far in non-multiple cases computation of the corresponding mains interference sample B_{2n+1} is according to Eq. (3), where B_0 and B_{-2n-1} are previous values of mains interference and B_F is the correction factor, represented by Eq. (4).

$$B_{2n+1} = 2B_0(2B_F - 1) - B_{-2n-1}, \tag{3}$$

$$B_F = \cos^2 \frac{\pi 2nF}{\Phi} \tag{4}$$

In multiple cases the correction is not necessary and the procedure for Z-filtering returns the corresponding sample of the mains interference without correction.

4. DSP REALIZATION

Our realization of the subtraction method is implemented by digital signal processor (DSP) of Analog Devices company – ADSP-2181, its common base architecture is optimized for digital signal processing and other high-speed numeric processing applications. The simulation is performed by Integrated Development Environment for ADSP-21XX. Integrated Development and Debugging Environment delivers efficient project management, enabling programmers to move easily between editing, building and debugging within a single interface.

In our algorithm from Fig. 2 the procedures for D-filter, (1-K)-filter and Z-filter are organized as separate modules. Each of these modules is called from main program with its input parameters and return the corresponding output values. This organization is very useful and permits of applying various types of D-, (1-K)- and Z-filters without changing the main structure of the algorithm.

There are two types of the buffer structure circular and linear-shifted. Circular buffer on Fig. 5 are faster than linear-shifted, furthermore the ADSP-21XX family base architecture includes hardware to handle address pointer wraparound, simplifying the implementation of circular buffers both on- and off-chip, and reducing overhead.

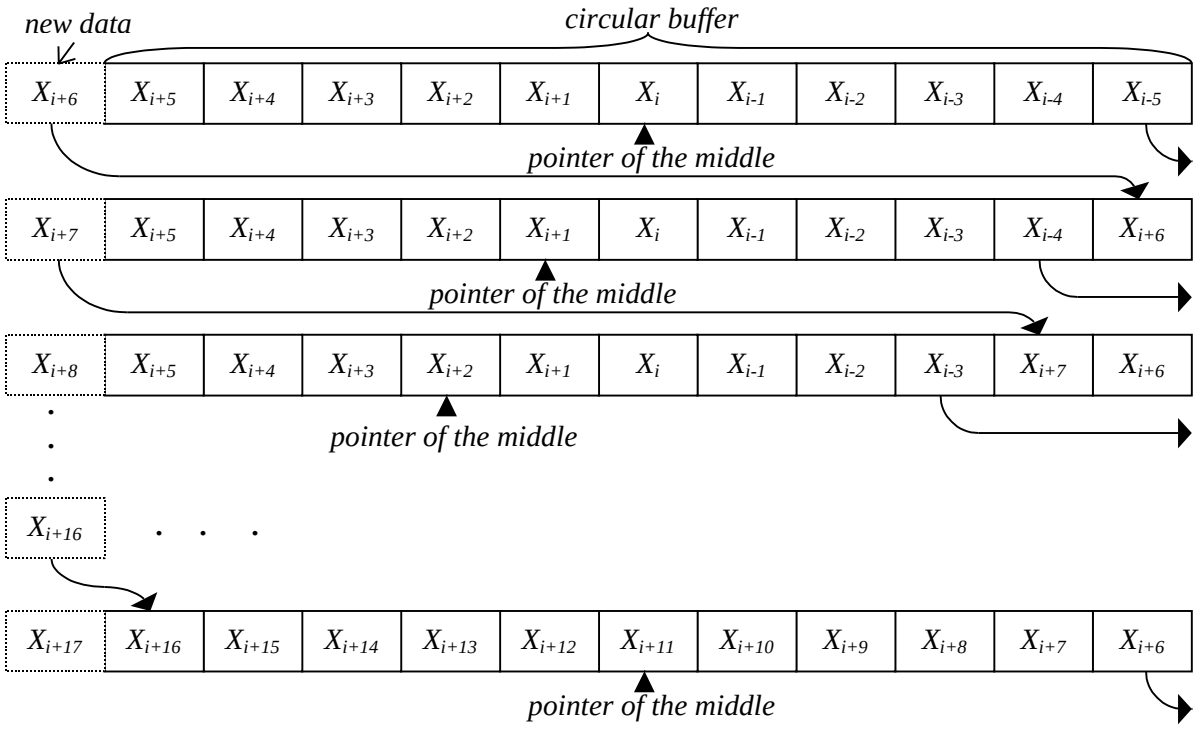

Fig. 5. Circular structure of the buffer

The buffers are located in data (DM) or program memory (PM). The data are fetched from DM or PM pointed to by corresponding index registers I0÷I7 and post-modified by the value in M0÷M7.

We have applied the subtraction method on various real electrocardiogram signals, taken from different patients, with heart diseases and healthy. These ECG are recorded from eight primary standard leads with Φ=250Hz sampling rate. The record length is 720 samples (2.5 sec.) per lead. The results of applying simple subtraction method are shown on Fig. 6. Curves a on Fig. 6 represent an ECG signal mixed with 50 Hz mains interference, curves b are the filtered ECG signals with sample moving average filter and curves c shown the error between original and filtered ECG signal.

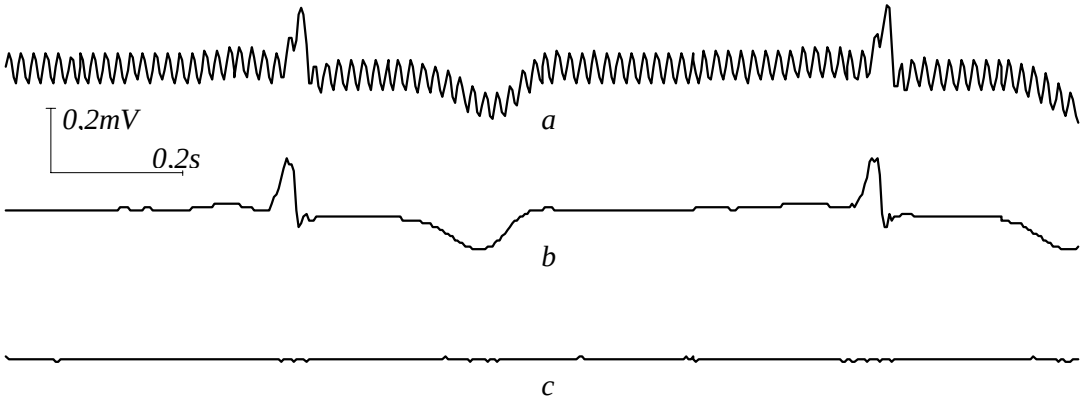

Fig. 6. ECG signal mixed with 50 Hz interference (a) and passed through the subtraction method (b). The error between original and filtered signal (c)

It is obviously that filter successfully eliminates 50 Hz interference, with minimum errors, only slight heights appear at QRS complexes and any high and abrupt waves.

5. CONCLUSIONS

In this article we described the subtraction method for removing mains interference from ECG signals and realized its algorithm in real time by DSP. Tree filtering procedures included in our algorithm are organized as separate modules, which permit us to apply various types of filters without changing the main structure of the algorithm. The running time of the program is very short. This is due to a multifunction operations take advantage of the inherent parallelism of the ADSP-21XX family architecture by providing combinations of data moves, memory reads/writes, and computation, all in a single cycle.

The fastness of the program is due to circular structures of the used buffers too. Furthermore the ADSP-21XX family base architecture includes hardware to handle address pointer wraparound, simplifying the implementation of circular buffers both on- and off-chip, and reducing overhead.

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