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ELEMENTS OF THE SILICON TCD DESIGN AND TECHNOLOGY

Key words: model, design, technology, silicon, detector

Silicon TCD (Thermal Conductivity Detector, katarometer) chip analytical model, elements of the design and technology are presented. Detector was designed for the μTAS (Micro Total Analysis System) application to recognize the composition of the different gas mixtures. TCD consists of the two pieces : glass plate and silicon chip. Two parallel flow channels 15 000 μm long, 400 μm wide and 50 μm deep were etched in the silicon chip and milled in the glass plate. Some of resistors were designed to act as a heaters and the other ones as a thermo resistors. Composition changes of the mixture flowing throughout the channel cause the temperature distribution changes and thermo resistors electrical response. Distance between the heaters and thermo resistors is of the great importance to the TCD sensitivity. VLSI silicon technology was applied to reduce geometrical dimensions and micromechanical technology to over-hange resistors across the flow channels to reduce thermal capacity and heat loses to the bulk and environment.

ANALYTICAL MODEL

Analytical model [1,2,3] is based on the heat transfer from the heater to the gas stream and environment. It can be expressed by the following second order differential equation (1). This model can be easily applied for the fast calculations even on the standard PC unit. One can estimate every individual parameter influence on the temperature distribution along the channel. Lost power (Q) from the heater to the TCD bulk and environment, caused by the resistor paths thermal conduction, were taken into account, too.

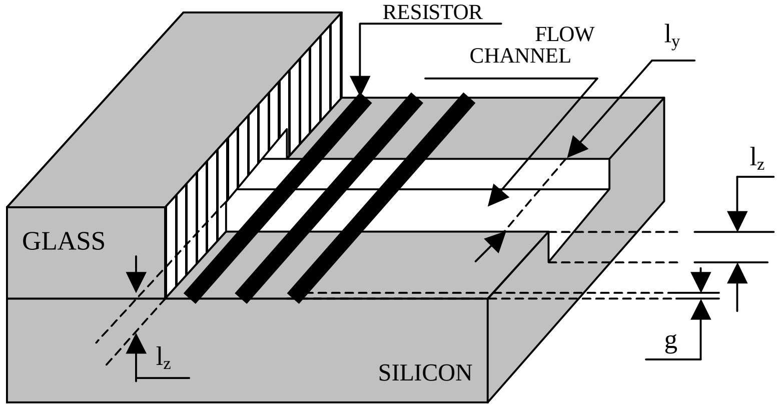


Fig. 1. Schematic semi cross-section of the TCD unit

$$\frac{d(P-Q)}{dx} = \lambda_f \cdot A \cdot \frac{d^2T}{dx^2} - \rho_f \cdot c_f \cdot A \cdot v \cdot \frac{dT}{dx} - 2 \cdot \lambda_f \cdot \frac{l_y}{l_z} \cdot T \qquad (1)$$

where:
$P = I^2 \cdot \rho \cdot n \cdot l_y / A_s$ – electrical power delivered to the heater, $Q = 4 \cdot \lambda_g \cdot A_s \cdot T_0 / l_y$ – lost power, x – parameter of the temperature distribution along the channel, I – heater current, ρ - heater material resistivity, n – number of the heater meanders, l_y – channel width, $A_s = w \cdot g$ – heater path cross section area, w – heater path width, g – heater path thickness, λ_g – heater material thermal conductivity coefficient, T_0 – heater temperature, λ_f – gas thermal conductivity coefficient, $A = 2 \cdot l_y \cdot l_z$ – channel cross section area, l_z – channel depth etched in the silicon chip and milled in the glass plate, T(x) – gas temperature inside the channel, ρ_f – gas mass density, c_f – gas heat capacity coefficient [2,3,4], v – gas flow rate (linear).

Solution of the equation (1), with several assumptions and boundary conditions, is given by [1]:

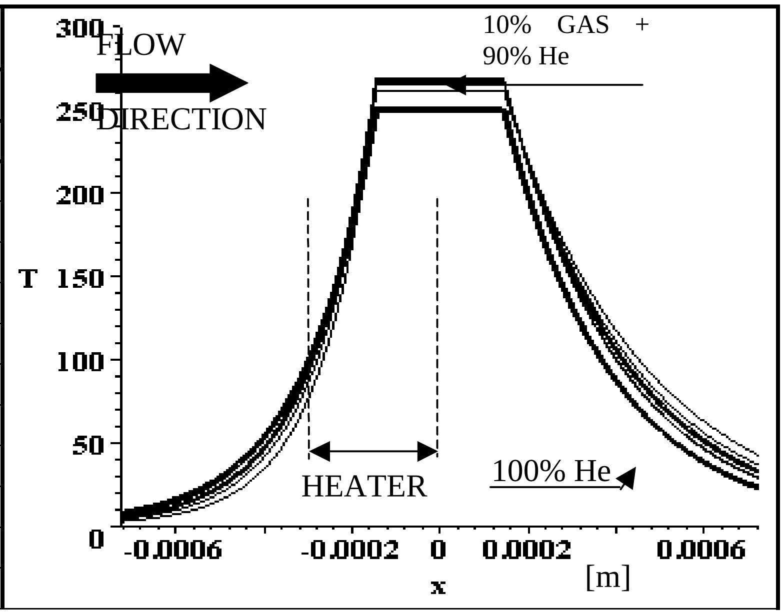
$$\begin{gathered} T_1(x) = T_0 \exp(\chi_1(x+L)) \ (x \le -L); \\ T_2(x) = T_0 \ (-L < x < L); \\ T_3(x) = T_0 \exp(\chi_2(x-L)) \ (x \ge L) \\ \chi_1 = \frac{1}{2 l_z A \lambda_f} \left(l_z v A c_f \rho_f + \sqrt{l_z A \left(l_z v^2 c_f^2 \rho_f^2 A + 8 l_y \lambda_f^2 \right)} \right); \\ \chi_2 = \frac{1}{2 l_z A \lambda_f} \left(l_z v A c_f \rho_f - \sqrt{l_z A \left(l_z v^2 c_f^2 \rho_f^2 A + 8 l_y \lambda_f^2 \right)} \right) \\ T_0 = \frac{I^2 \cdot \rho \cdot n \cdot l_y^2 \cdot l_z}{A_s \cdot \left(l_y \cdot l_z \cdot A \cdot \lambda_f \cdot \chi_1 - l_y \cdot l_z \cdot A \cdot \lambda_f \cdot \chi_2 + 4 \cdot l_y^2 \cdot \lambda_f \cdot L + 4 \cdot l_z \cdot \lambda_g \cdot A_s \right)} \end{gathered} \qquad (2)$$

where $L = n \cdot w + (n-1) \cdot s$ is the heater length along the channel, s – is the heater meander paths separation, and χ_1 and χ_2 are the coefficients.

Assuming that the thermal parameters of the mixture are proportional to the percentage, gas temperature at the TCD inlet is 0^oC as well as the heater current **I** is 15 mA, gas mixture flow rate **v** is 0.3 m/s, gas concentration of each gas is 10 % in He, geometrical dimensions are **g** = 1 µm, **w** = 30 µm, **n** = 3, $\mathbf{l_y}$ = 400 µm, **L** = 145 µm, one can easily calculate (2) the heater temperature and the temperature distribution along the channel (Table 1).

Tab.1. Calculated temperature of the heater and distribution along the channel.

Gas	T_0 [°C]
100% He	249.6
10% C_2H_6 +He	266.8
10% C_2H_2 + He	267.6
10% N_2 +He	266.4
10% SO_2 + He	260.6
10% CO_2 + He	264.6
10% C_2H_4 + He	267.4
10% CH_4 + He	267.2
10% H_2O + He	268.1
10% CO + He	266.6
10% H_2S + He	267.1
10% O_2 + He	265.6



2. DESIGN

Detector consists of the two elements: silicon chip and glass plate (Figure 1), [8]. Glass plates (15mm × 15mm × 2mm) were formed with use of standard mechanical milling and dicing technique. Silicon chips (15mm × 15mm × 0.39mm) were fabricated with use of the VLSI technology, supplemented by the several MEMS-typical steps. Two identical resistor sets were patterned on the silicon chip - one inside the measurement channel, the other in the reference channel. Resistors were formed from the phosphorous doped polysilicon layer 0.5μm-thick, or from the platinum layer 0.25μm-thick. They were arranged in the meander lines 30μm-wide, along the {110} directions of the mono-crystalline substrate. Several different resistor lengths, according to the Figure 2, can be electrically connected to the package output ports (2-3)=(3-4)=(4-5) = 2000μm, (1-2) = 7200μm. Two phosphorous doping levels of the polysilicon layer were applied : U/I=1.72Ω (R_S≈8Ω/□) and U/I=3.4Ω (R_S≈16Ω/□). Each resistor has individual electrical outputs through the contact windows in the dielectric layers, through the diffusion paths (n^+), through the BSC-type contacts, to the external bonding pads, located on the opposite side of the silicon chip.

3. ELEMENTS OF THE TCD TECHNOLOGY

3.1. BSC-type contacts formation

Resistors electrical connections to the bonding pads were designed with use of the back-side-contacts (BSC) [5]. This type of contacts allow the resistor positioning on the one side of the silicon chip and the bonding pads on the other. BSC formation requires very deep substrate etching and doping, so it should be done at the beginning of the technological sequence. SiO_2 and Si_3N_4 masking layers were damaged after the BSC formation and have been replaced by the new ones. The first photolithography was done to define BSC shapes in the masking layers. KOH-water solution was used for the (100) silicon substrate anisotropic etching. During this step deep, square groves with the (111) sidewalls and (100) bottom, closed by the 20-30μm-thick membranes, were formed. Second photolithography defined regions to be phosphorous doped (n^+-type) on the opposite side of the silicon substrate (p-type). To connect diffusion paths from one side to the other, junction depth should be x_j = 11-16 μm, depending on the membrane thickness.

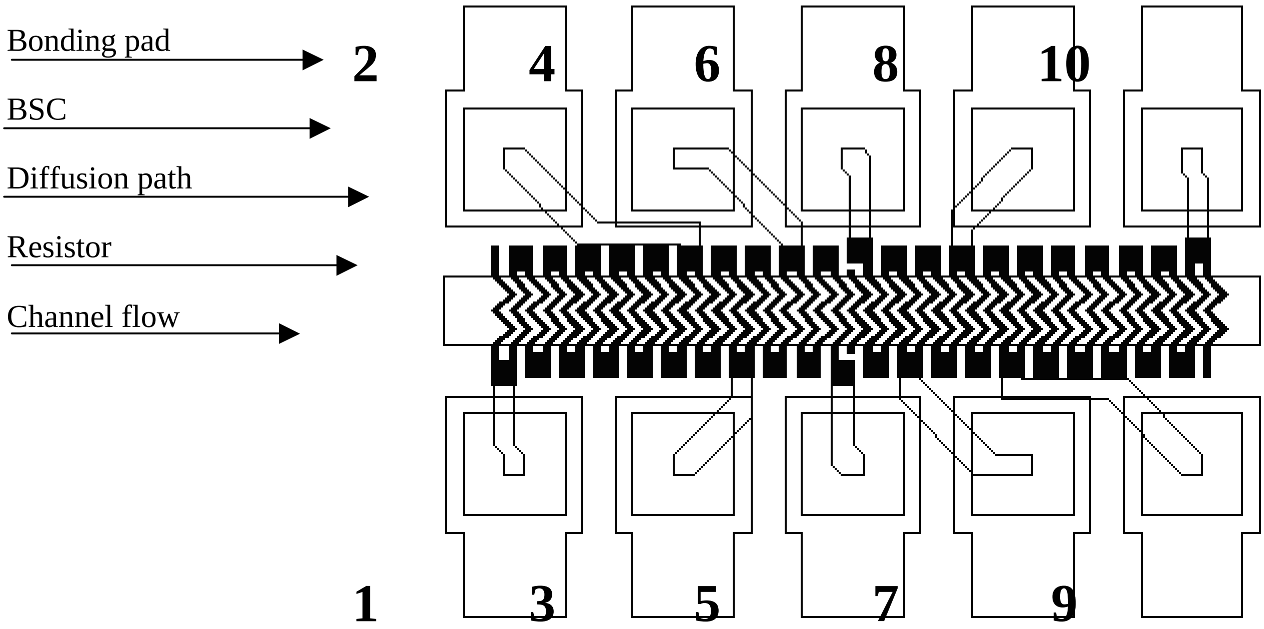


Fig. 2. TCD resistors arrangement

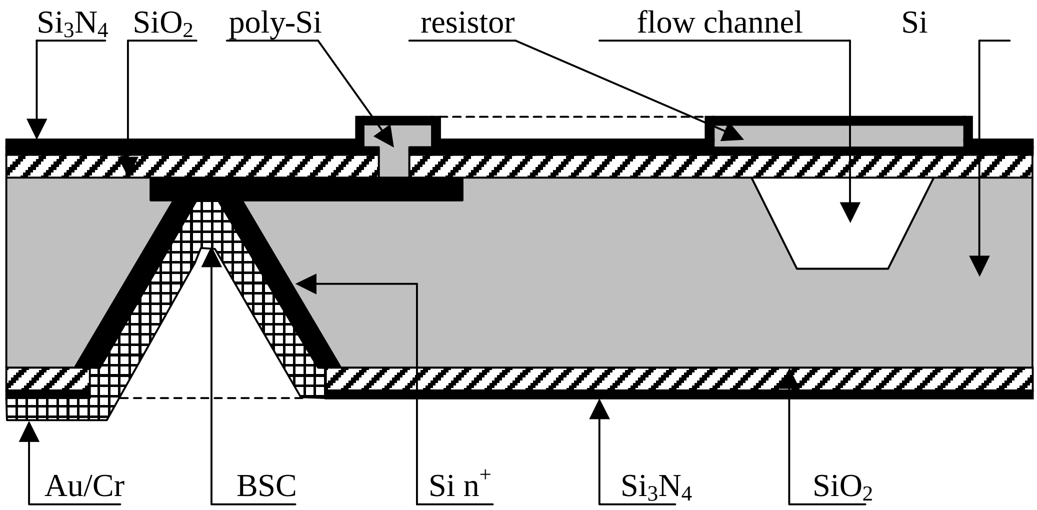


Fig. 3. TCD silicon chip schematic cross-section

Next technological steps were performed on the wafers with the high aspect ratio. This caused several problems during the subsequent photolithography steps: resist spin-on non-uniformity and edges low quality, light reflections from the BSC side-walls (111) crystal planes and vacuum chucks performance deterioration. BSC surface was covered by the thin Cr layer (for better adhesion) and Au layer (typical bonding pad material, also resistant to the TMAH-water solution). This step required application of the negative and positive thick photoresists and two similar masks with slightly different shape dimensions (to compensate underetch phenomena). First – for the dielectric layers removal from the BSC groves; second – for the Cr/Au sandwich bonding pads formation and BSC walls perfect covering, Figure 3. Negative photoresist ma-N-1420 required exposure dose 550 mJ/cm^2 and positive one ma-P-100 dose 400 mJ/cm^2. These parameters were decisive for the satisfactory final result. Si_3N_4 layer was plasma etched, SiO_2 layer was chemically etched in the HF: NH_4F solution, Au layer was etched in the thiocarbamide solution, and Cr layer in the ammonium-cerium, acetic acid water solution.

3.2. Resistor formation

Resistor formation phase depends on the resistor material. Experiments were done with phosphorous doped poly-silicon and platinum [6,7]. At the beginning contact windows were opened in the dielectric layers on the silicon substrate. Poly-silicon layer was deposited in the LPCVD-type chemical reactor, doped from the PSG layer (phospho-silicate-glass) and formed into the resistor shapes with use of the standard (chemical etching only) photolithography step. To form platinum resistors lift-off technique was applied. Both Pt and poly-Si resistors were covered by the plasma silicon nitride layer – of good masking properties against the TMAH-water etching solution.

In the final photolithography step flow channels were defined in the photoresist layer and SiO_2/Si_3N_4 layers. Wafers were diced into the individual silicon chips. Channel etching was performed in the TMAH-water solution at 80^oC for 200 minutes. This solution have a little worse anisotropic coefficient than standard KOH-water solution, but it doesn't attack most of metal layers and the etch rates of the plasma Si_3N_4, LPCVD Si_3N_4 and thermal SiO_2 layers are negligible. Special orientation of the channel mask shapes aligned to the {110} directions gives convex corners with [310] crystal planes of high etch rates. This design accelerates masking layer under-etching in desired direction and individual grooves aggregation into one channel shape.

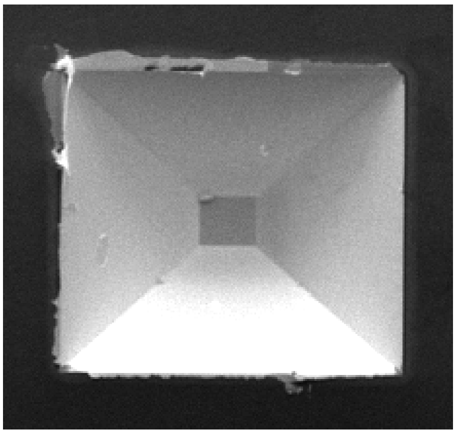


Fig. 4. SEM of the BSC covered by the Cr/Au layers

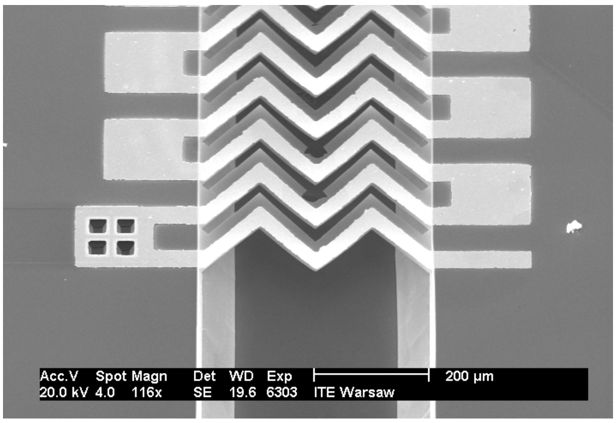


Fig. 5. SEM top view of the flow channel with the fragment of the Pt resistor

4. RESULTS

TCD silicon chips were fabricated with Pt or poly-Si resistors and BSC-type electrical outputs. Chips were bonded with the glass plates with corresponding grooves mechanically milled on the surface. Gas tubings were attached with use of the waterproof glue to the channel outlets and bonding pads of the TCD were electrically connected to the bonding pads of the package. Standard ultra-thermo-compression method was used. Initial electrical tests of the TCD device have confirmed sensitivity to the flow and gas composition changes.

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OPTICAL LINKS OF DATA TRANSMISSION IN CITY AREAS

Modernly produced optical links of data transmission, which are working in an opened waether area on infrared waves, are used as links of data transmission in cities. Optolines are used for fast construction of connections on distances ranging from tens of meters to several kilometers. They are used to transmit bit rates of 2Mbit/s or n*2Mbit/s.

The article presents the operational estimate of usefulness of the optoline working on waves of λ = 0,86 - 0,92µm spectral range. Despite low estimates of the product a new prospect appears before it. New technologies enable optolines to work on waves of λ = 9 - 12µm spectral range and are the future for evolution of that practical device.

The article also speaks of expectations in the subject of transmission parameters.

1. INTRODUCTION

The need for telecommunication services in large cities is growing rapidly. Telecommunication systems in these areas often need reconstruction, but these are very costly and long lasting operations because they interfere with the technical structure of the cities. They