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THERMAL RESIDUAL STRESSES IN THICK FILM STRUCTURES RESISTOR ON DIELECTRIC – FEM ANALYSIS

This paper presents the results of calculations performed using the finite element method (FEM) which include a comparative analysis of residual stress state induced in thick film structures resistors on dielectrics which differ from one another in materials used to perform dielectric layers. This analysis permitted us to test the materials examined in terms of the level and distribution of the residual stresses developed in the structure.

1. INTRODUCTION

Miniaturisation in thick film microcircuit is realized by higher density packaging of elements. It could be achieved by producing closer paths and/or producing more levels in the multilayer structure. Introducing resistors to the multilayer structures always causes problems.

The simplest alternative is to a pre-completed multilayer structure as a substrate for resistor deposition, which becomes the last layer to be printed and fired. This reduces the number of resistor firings to one and eliminates level changes. It is necessary to find sufficiently large flat areas for resistor deposition. This configuration allows the laser trimming of resistors. But this method has also some disadvantageous. The pastes used must be very carefully selected. Most of standards resistive do not react with dielectric layer in the same way as with alumina [1, 2]. In some cases the interaction of dielectric with resistor is significant [3, 4].

From the other hand, when the miniaturisation of the devices takes place, problems with thermal management becomes a very significant problem. When there is a sequence of different layers in the structure, the compatibility (in respect of thermal expansion coefficient) of the layers without generating considerable stresses becomes a very important problem.

This paper presents the results of calculations performed using the finite element method (FEM) which include a comparative analysis of residual stress state induced in Thick film structures resistors on dielectrics which differ from one another in materials used for dielectric layers. This analysis permitted us to test the materials examined in terms of the level and distribution of the residual stresses developed in the structure.

2. DESCRIPTION OF STRUCTURE RESISTOR ON DIELECTRIC

The simplest structure which we have defined as resistor on dielectric (R-D) investigated in this paper is as follows The structure placed on 96 % alumina substrate was obtained by screen-printing and firing in air atmosphere the following layers:

- dielectric layer,
- conductive layer for resistor terminations,
- resistive layer.

The scheme of this structure is presented in Fig.1.

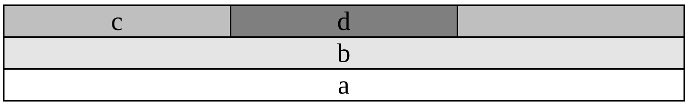


Fig. 1. The scheme of the simple structure resistor on dielectric.
a – alumina substrate, b – dielectric layer, c – resistor terminations, d – resistive layer

The test pattern used for this investigation is shown in Fig.2. The alumina substrate (96% Al_2O_3) produced by CeramTec was 2x2 inches large and 0.63 mm thick. Two different dielectric layers were screen-printed on the substrate, one was D-421 (ITME)[5], the other one was c-BN based dielectric layer [6]. Both tests with the layers were fired at 850^{o}C, and then a resistor with its termination was deposited by the use of standard thick film process.

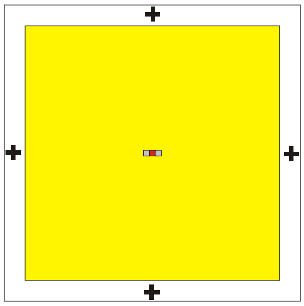


Fig. 2. Test pattern used in this investigation

Palladium silver P-202 (ITME)[7] and a resistive one based on ruthenium dioxide and lead-silica-aluminium glass was chosen to elaborate the structure resistor on dielectric [8].

For comparison, a structure where resistor was placed on bare alumina substrate was also prepared.

3. ASSUMPTIONS ADOPTED IN CALCULATING THE RESIDUAL STRESSES

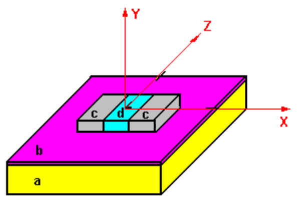
The models of thick film resistor on dielectric structures used for the three dimensional analysis with the use of finite element method (FEM)[9] is presented in Fig.3.

The analysis of the stress sate in the examined structures was made based on the assumptions:

- the materials examined show isotropic properties,
- the phenomena occurring in the materials show only thermo-elastic character.

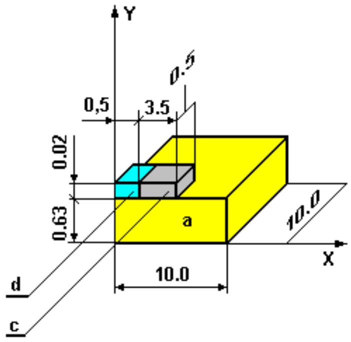
An example of the finite element mesh for 3 D model into which the model resistor – substrate without the dielectric layer is presented in Fig.4. The net was divided into 7414 cubic elements connected with 8925 nods. This is one forth of the real structures, but since the structure is symmetric this is enough for the analysis.

The materials parameters, such as the thermal expansion coefficient α, Young's modulus E, yield stress Re and the Poisson ratio ν, used in the calculations are listed in Table 1. The parameters were temperature- dependent, except the Poisson ratio which was assumed to be temperature-independent



a - substrate,
b -dielectric layer (b1- D-421 or b2- c-BN),
c - conductive layer, d- resistive layer

a)



b)

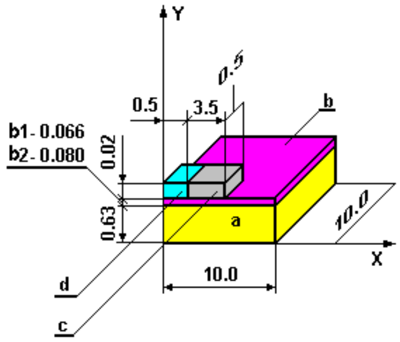


Fig. 3. The model of the structure resistor-dielectric used in finite element calculations of thermal residual stresses, (a) - without the dielectric layer, (b) – with the dielectric layer

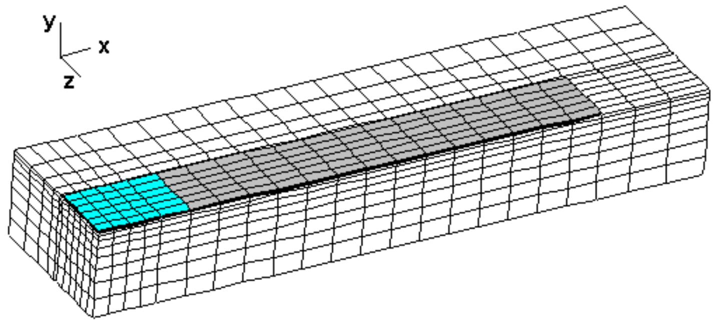


Fig. 4. Enlarges part of finite element mesh used for the numerical analysis of residual stresses of structure resistor – substrate (without dielectric layer)

Table 1

Material properties (at room temperature) used in the calculations of thermal residual stresses [10,11].

Type of material	**E (GPa)**	**Re (MPa)**	**α (*10^{-6}/^{o}C)**	**ν**
Substrate Al_2O_3	341	-	6.3	0.22
Dielectric layer D-421	74.3	-	4.1	0.22
Dielectric layer (c-BN)	642.2	-	3.15	0.38
Conductive layer	77.4	-	16.26	0.33
Resistive layer	196.9	-	7.84	0.24

The load imposed on the analysed models is associated with the process of producing the structures. The main factor generating the stresses in the investigated structures are the changes of temperature. The decrease of temperature during the firing process (cooling of the sample) together with the difference of properties (Δα, ΔE) of the materials used to prepare the structure result in residual stresses being induced to the structure. It has been assumed that the residual stresses develop in the system during its cooling from 700^{o}C, when the glass is spreading in layer to 20^{o}C (room temperature).

4. RESULTS AND DISCUSSION

The numerical calculations gave maps of the thermal residual stress distribution and the values of the central region of elements. The program permitted calculating the following components of the stress state: axial stresses S_z, S_x, S_y, tangential stresses S_{xy}, S_{yz}, S_{xz}, and principal stresses S1, S2, S3 (max or min).

From the calculations of the thermal residual stresses we can observe that the highest level of stresses exhibit the main stresses S1 (Fig.5). In the maximum concentration area of the stresses is located in the resistive layer close to the interlayer between the resistive and conductive layer. The stresses S1 exhibit the stretching character with maximum value of 71MPa in the model without dielectric layer and of 72MPa with dielectric layer D-421 and 80MPa with dielectric layer c-BN (see Table 2).

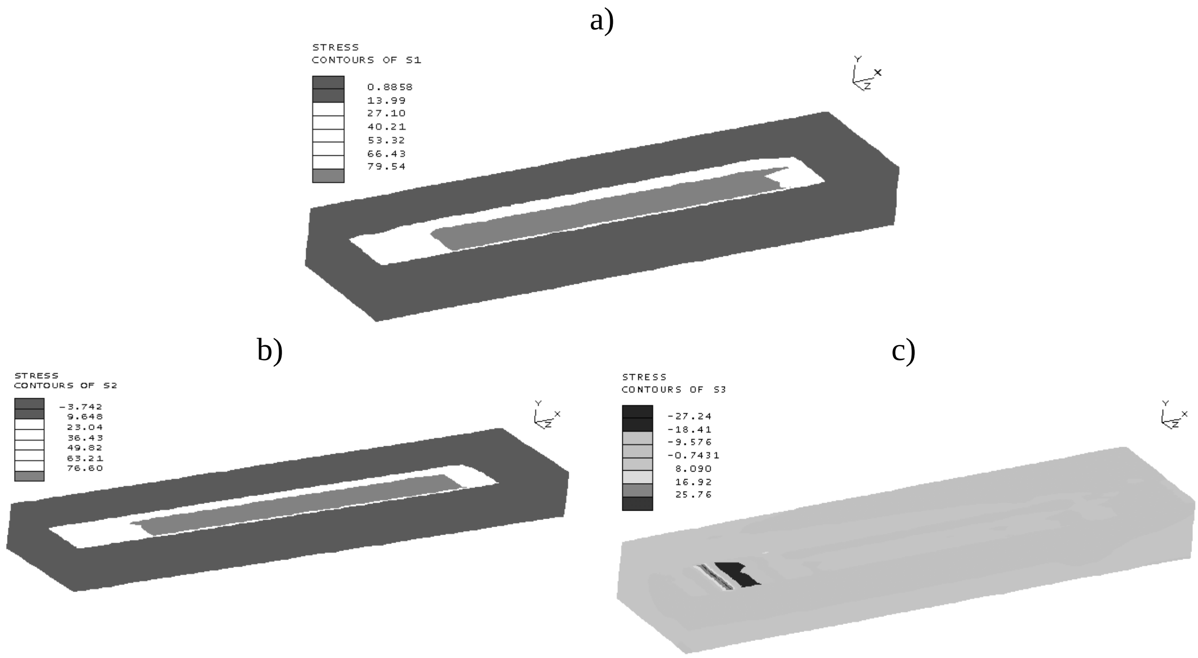


Fig. 5. Map of distribution of principal stresses S1 (a), S2 (b), S3 (c) in the model of the structure resistor-dielectric. (Stress value in MPa)

Table 2

Maximum values of the principal stress S1 inside the resistive layer in the model of the structure resistor-dielectric calculated by FEM.

Model of the structure resistor-dielectric	**Stress S1 (MPa)**
without dielectric layer	71
with the dielectric layer D-421	72
with the dielectric layer c-BN	80

Examples of distribution of main stresses S1 along the chosen cross sections of the model with and without the dielectric layer are presented in Fig. 6-8.

a b

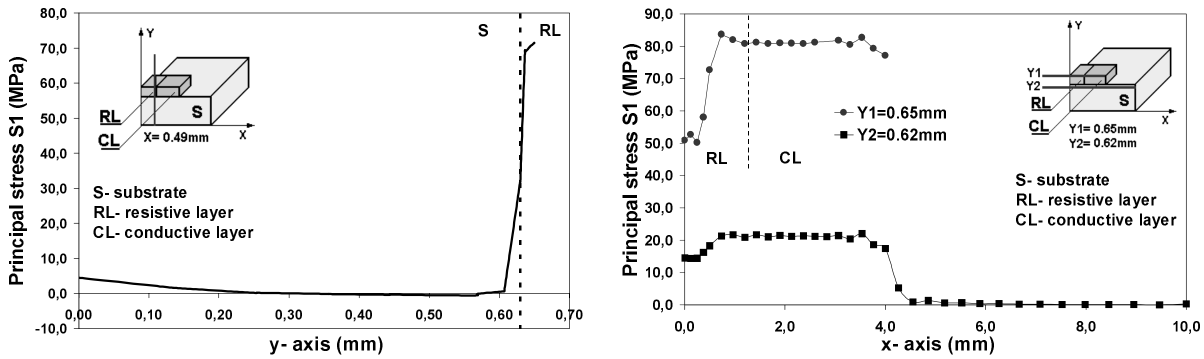


Fig. 6. Distribution of the principal stress S1 in the model of the structure resistor-dielectric, without the dielectric layer: a) along y- axis for x= 0.49mm, b) along x- axis for y1= 0.65mm and y2= 0.62mm

a b

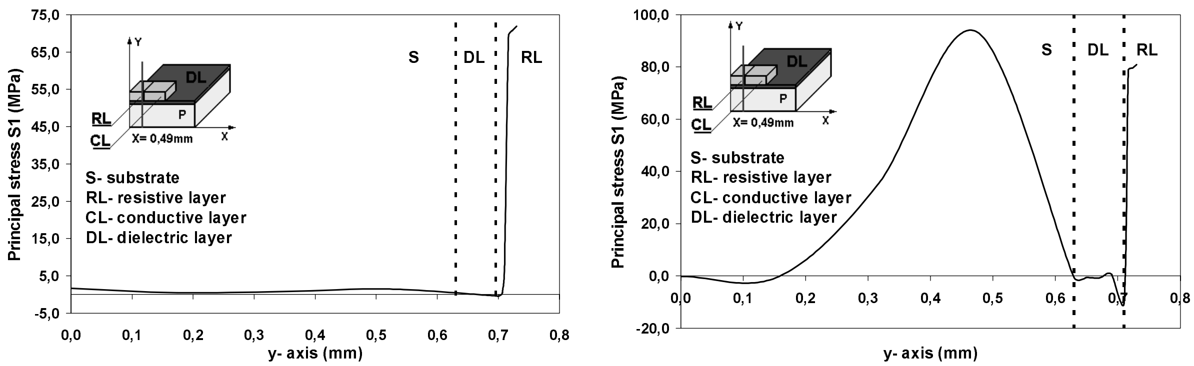


Fig. 7. Distribution of the principal stress S1 along y- axis for x= 0.49mm in the model of the structure resistor-dielectric, with the dielectric layer a) D-421, b) c-BN

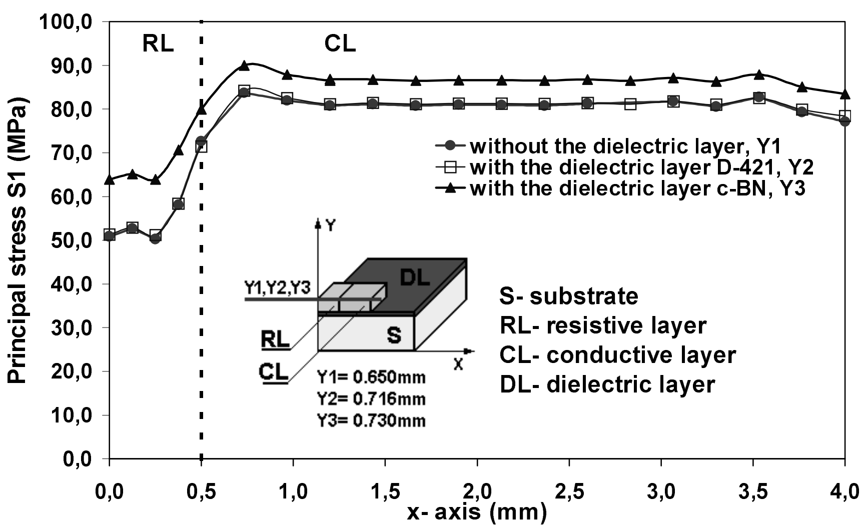


Fig. 8. Comparison of the principal stress S1 distribution along x- axis for selected y section in the model of the structure resistor-dielectric without and with the dielectric layer

5. CONCLUSIONS

The results obtained from the numerical calculations for the models for resistors situated on different dielectric layers showed that the thermal residual stresses in the resistive layer are comparable with the stresses when the resistor is situated on bare alumina substrate. That means that the dielectric layers are compatible with the resistive layer.

The stresses show the stretching character. This stays in agreement that the higher value of stresses the resistor exhibit higher value of resistivity [8].

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