# The Heat Treatment Influence on the Main Quality Indicators of Ag/n-n<sup>+</sup>GaAs Heterojunctions

Vadim Dmitriev<sup>1</sup>

1. Microelectronic information systems department, Zaporizhzhya State Engineering Academy, UKRAINE Zaporizhzhya, Soborny Ave., 226, E-mail: dems562@gmail.com

Abstract – The effect of heat treatment on the parameters and characteristics of  $Ag/n-n^+GaAs$  heterojunctions is studied. Various methods for the Schottky barrier height and the nonideality factor determining have been examined and tested. The most accurate method for determining the heterojunction parameters using the current-voltage characteristic was found. Keywords – heterojunction, current-voltage characteristic, barrier height, nonideality factor, silver.

#### I. Introduction

The study of silver-gallium arsenide heterojunctions is carried out in the direction of the technological regimes development which can improve the qualitative characteristics of microwave devices with Schottky barriers [1, 2]. Comparing to gold, silver has a higher thermal and electrical conductivity, a relatively small diffusion coefficient in gallium arsenide, which allows to reduce the transition layer thickness. This should improve the products technical characteristics. Therefore, the technological regimes development to manufacture improved silver based GaAs heterojunctions is relevant from a scientific and practical poinst of view.

The aim of current work is to determine the heat treatment influence on the real current-voltage characteristics, the Schottky barrier height  $\phi_b$  and the nonideality factor  $\eta$  of the Ag/n-n<sup>+</sup>GaAs heterojunction.

# II. Matherials And Methods

For the study, n-n<sup>+</sup>GaAs (111) B epitaxial monocrystalline was used, the epitaxial layer thickness was 2  $\mu$ m, the donor concentration was N<sub>D</sub>=2·10<sup>16</sup> cm<sup>-3</sup>. The GaAs substrate was degreased in a mixture of toluene and methyl alcohol (1:2), treated in H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O:3:1:1 sulfuric acid etchant, followed by exposure to dioxisuccinic acid during 1.2·10<sup>3</sup> seconds.

According to the results of previous studies [1-2], highpurity silver is chosen as the barrier material. With GaAs it forms compounds that do not change in the operating temperature range. The contacts were made by vacuum evaporation. To measure the metal-semiconductor barrier transition current-voltage characteristics (CVC) a fourprobe method has been used [3].

The thin-film structures with a Ag/n-n<sup>+</sup>GaAs Schottky barrier current-voltage characteristics analysis assumed, that in the initial structures the charge carrier transfer mechanism at the free carriers concentration  $N_D=2\cdot10^{16}$  cm<sup>-3</sup> in GaAs is determined by thermionic emission.

Despite the fact that the basic physical processes in the Schottky barriers have been studied in [4] and [5], there

are still some disagreements about the the current-voltage characteristics deviation reasons from the ideal ones. It is assumed [5] that the real metal-semiconductor barrier transitions CVC depend on the their fabrication method. One of the main qualitative indicators of such contacts are barrier height  $\phi_b$  and nonideality factor  $\eta$  [4] and [5], however the accuracy of these parameters depends not only on the accuracy of current and voltage measurement, but also on their determination method.

The comparative analysis of the Schottky barrier height  $(\phi_{bn})$  is made of the determining methods accuracy using the CVC, based on the experimental data obtained for Ag/n-n<sup>+</sup>GaAs barriers.

There are several methods for the potential barrier height  $\phi_b$  determining [4,5,6]. the  $\phi_b$  determining method from the CVC direct branches is one of them [4,5].

In [5] authors described the current-voltage characteristic, taking into account the limitation of the describing the steady-state CVC to four parameters (Schottky barrier height,  $\phi$ , nonideality factor  $\eta$ , successive  $R_s$  and shunt  $R_p$  resistances) as Eq. 1:

$$I = I_0 exp\left(\frac{qV_{pn}}{\eta kT}\right) \left[1 - exp\left(\frac{-qV}{kT}\right)\right] + \frac{V_{pn}}{R_p}$$
(1)

where  $I_0=A^{**}T^2Sexp(-q\varphi_b/kT)$  is the saturation current,  $V_{pn}=V-IR_s$  is the voltage at the metal-semiconductir transition,  $R_p$  – shunting resistor; Ohm;  $R_s$  – flow resistance, Ohm;  $A^{**}$  – the effective Richardson constant,  $A \cdot cm^{-2} \cdot K^{-2}$  and S is the area of contact,  $cm^2$ .

From the Eq. 1, the conditions [5,7] were determined. There the contribution of  $R_s$  and  $R_p$  is very small (less than 1%) and they can be neglected:

The calculation of the CVC by the method proposed by Rhoderick E.H. in [5] is the simplest in the implementation. The current through the Schottky barrier is described there by the Eq. 2:

$$I = I_0 exp\left(\frac{qV}{\eta kT}\right) \left[1 - exp\left(\frac{-qV}{kT}\right)\right]$$
(2)

Here V is the applied voltage, V;  $\eta$  – non-ideal factor; T – the environment temperature, K; q – the electron charge, Kl; k is a constant. In [7-10], the direct approximation method for the entire CVC length is proposed and described by the Eq. (1). The disadvantage of this method is the complex calculations.

# **III.** Experiment

The current-votage characteristics of Ag/n-n<sup>+</sup>GaAs heterojunctions, which were made in vacuum by the thermal evaporation method at annealing temperatures of 703...853 K and an annealing time of  $6 \ 10^2$  seconds were investigated, Fig. 1.

The main parameters calculation of the produced at different temperature regimes Ag/n-n<sup>+</sup>GaAs heterojunctions (Table 1) was made using the IVbarrierCalc2 program [7].

It is established that an annealing temperature increase up to 803 K gives the highest barrier height  $\phi_b$  for the Ag/n-n<sup>+</sup>GaAs heterojunction.



TABLE 1 THE AG/N-N<sup>+</sup>GAAS HETEROJUNCTIONS PARAMETERS

t <sub>ann</sub> , K	The calculation method	η	φ <sub>b</sub> , V	R <sub>s</sub> , Ohm	e
703	direct approx.	1,254	0,773	0,21	0,28
	Rhoderick	1,20	0,783	-	0,09
753	direct approx.	1,24	0,804	0,75	0,31
	Rhoderick	1,30	0,800	-	0,44
803	direct approx.	1,08	0,983	3,70	0,07
	Rhoderick	1,10	0,979	-	0,07
853	direct approx.	1,32	0,85	1,02	0,3
	Rhoderick	1,34	0,85		0,29

## IV. Discussion

A comparative analysis of the obtained nonideality factor  $\eta$  values (Table 1), calculated by two different methods, showed that for barrier silver to GaAs based transitions with  $N_D{=}10^{16}~{\rm cm}^{-3}$ , produced by the recommended heat treatment method (the annealing temperature is 803 K, the annealing time is 6  $10^2$  seconds,  $\phi_b{=}0.98~V$ ), the smallest nonideality factor value of  $\eta{=}1,104$  is obtained using the direct approximation calculation method. The [4] and [5] explain that the nonideality factor  $\eta$  at a low doping level ( $N_D{=}10^{15}~{\rm cm}^{-3}$ ) and 300 K is close to 1, but with the doping level increase ( $N_D{=}10^{16}~{\rm cm}^{-3}$ ), the difference of  $\eta$  from 1 becomes significant.

Studies show that in order to determine the height of the potential barrier for a short extension of the exponential CVC part, the direct approximation method is the most accurate, since it takes into account the series resistance and the C-V characteristic for V < kT/q.

The nonlinear  $\phi_b$  nature dependence of the applied voltage appears in the displacements bounded in region between 0.44...074 V (Fig. 1), which leads respectively to a nonideality factor  $\eta$  change.

#### Conclusion

It has been established that the annealing temperature increase to 803 K gives the highest value of the barrier height  $\phi_b$  for the Ag/n-n<sup>+</sup>GaAs heterojunction. Using this

recommended thermal processing regime forf the Ag/nn<sup>+</sup>GaAs barrier transitions (annealing temperature of 803 K during 6 10<sup>2</sup> seconds), the least nonideality factor value  $\eta = 1,087$  was obtained by the direct approximation calculating method. The nonlinear nature of the dependence of the barrier height  $\phi_b$  on the applied voltage appears in the displacement region bounded between 0.44 ... 074 V, which respectively leads to a change in the non-ideal factor  $\eta$ . With a short extension of the exponential region of the CVC to determine the height of the potential barrier, the most accurate direct approximation method used, since it takes into account the serial resistance and the CVC region at V <kT/q.

## References

- P. Jayavel, J. Kumar, P. Ramasam, R. Premanand, "On the evaluation of Schottky barrier diode parameters of Pd, Au and Ag/n-GaAs", Indian Journal of Engineering and Materials Sciences, Vol. 7, №5-6. – pp. 340–343, 2001.
- [2] Dmy`triyev V.S. "Inzhektuyuchi bar'yerni perehody` na osnovi arsenidu galiya dlya pry`ladiv NVCh diapazonu" Progresy`vni texnologiyi ta pry`lady`, № 10(1), pp. 50-53, 2017.
- [3] A. V. Belyaev, N. S. Boltovecz, E. F. Venger y`dr., "Fy`zy`chesky`e metodi dy`agnosty`ky` v my`kro- y` nanoelektrony`ke", Khar`kov, Y`SMA, 284 p., 2011.
- [4] S. M. Sze, K. K. Ng "Physics of Semiconductor Devices, 3rd Edition", Hoboken, A John Wiley & Sons, Inc., 815 p., 2007.
- [5] E. H. Rhoderick, R. H. Williams, "Metal-Semiconductor Contacts", Oxford, Clarendon Press, 252 p., 1988.
- [6] S. Chand, L. Kamar, "Origin of non-ideal currentvoltage characteristics of metal-semiconductor contact: A numerical study", Indian Journal of Engineering & Materials Sciences. Vol. 7, № 5-6. pp. 268–273, 2000.
- [7] Kudryk Ya.Ya., Shynkarenko V.V., Slipokurov V.S., Bigun R.I., Kudryk Ya.Ya, "Methods for determination of Schottky barrier height from I-V curves", CriMiCo'2014, September 7-13, Sevastopol, Crimea, pp. 673-674. 2014.
- [8] M. P. Hernández, C. F. Alonso, J. L. Peña, "Barrier height determination in homogeneous nonideal Schottky contacts", Journal of Physics D: Applied Physics, Vol. 34, №8, pp. 1157–1162, 2001.
- [9] N. Karaboga, S. Kockanat, H. Dogan, "The parameter extraction of the thermally annealed Schottky barrier diode using the modified artificial bee colony", Applied Intelligence, Vol. 38, № 3. pp. 279–288, 2013.
- [10] A. Ortiz-Conde, Y. Ma, J. Thomson, etc, "Direct extraction of semiconductor deviceparameters using lateral optimization method", Solid-State Electronics, Vol. 43, №4. pp. 845–848, 1999.

INTERNATIONAL YOUTH SCIENCE FORUM "LITTERIS ET ARTIBUS", 23–25 NOVEMBER 2017, LVIV, UKRAINE 403