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Speed analyse of two step algorithms of trigonometric transformations on multi-core processors

Keywords: *DCT, FCT, trigonometric transformation, multi-core processor.*

Abstract

The two-stage trigonometric transformations algorithms are based on calculations divided into two parts, in which operations of addition and subtraction are performed, as well as, at one stage, operations of multiplication. Since the algorithm graph resembles the Fourier transform graph, it is possible to make such a decomposition of the graph which enables to extract a group of elements on which calculations are performed in the same way. By appropriate substitution of addresses assigned to input data and particular steps the corresponding values for the cosine and sine for multiplication operations, we can achieve full symmetry calculations for each step of the algorithm. Such algorithm may be subjected to any decomposition allowing to split the process of the calculations into any number of processes, which can be implemented independently within one step of the algorithm. Additionally, a single step of algorithm may depend on the size of the data and the associated number of arithmetic operations, which implementation may depend on available hardware resources. Example graph for four point computational blocks is shown in Figure 1.

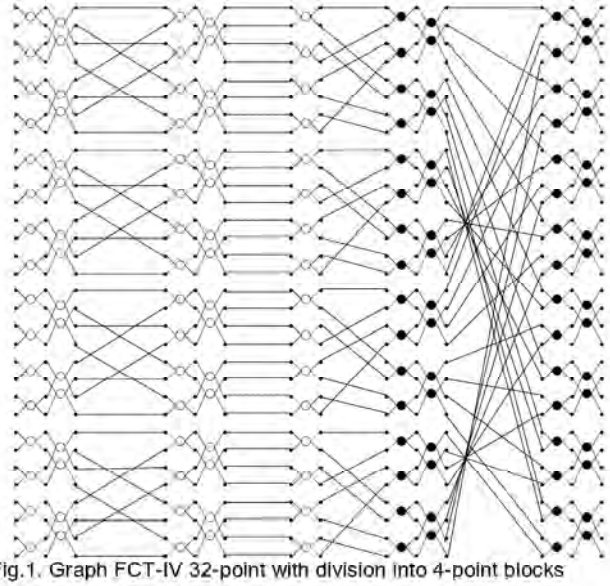


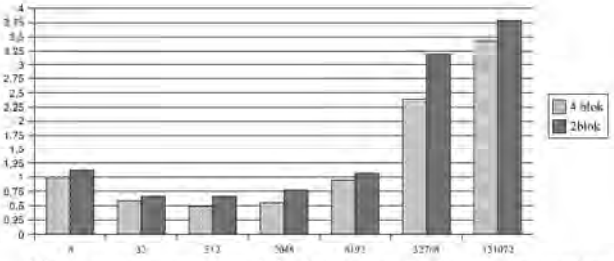
Fig.1. Graph FCT-IV 32-point with division into 4-point blocks

The implementation of block processing technique allows to reduce the number of indirect references to the operating memory of a computer. As the speed of downloading data to and from computer's memory is much slower than the numerical calculations in numerical coprocessor, the application of the method grouping butterfly calculating in blocks of 4-point rate increase the speed of the calculations of about 10% in comparison to the classical 2-point butterfly algorithm used in PC-class processor (Intel Celeron). The increase in the speed of calculation is dependent on a particular processor architecture. 64-bit processors of PCs class have been enriched by additional fast internal registers which allow to increase the size of calculation block. Multi-core and multi level system of processor cache memory can be expected to further affect the increased speed of multipoint computing of trigonometric transformations.

It is advisable to compare the speed of calculation algorithm on multi-core processors using parallel computing for different sizes of trigonometric transformations.

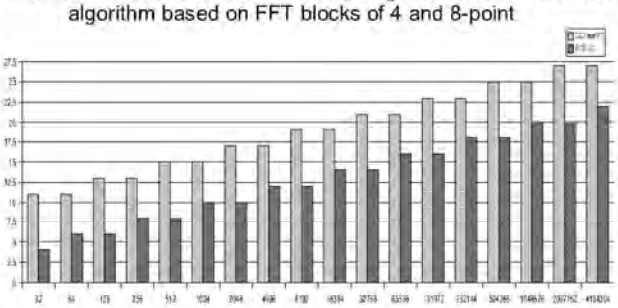
The increase of the speed of calculation associated with increasing of block calculation rate from 2 to 4 points is presented in Table 1.

Table 1. Computation time FCT-IV algorithms of blocks of 2 and 4-point



The maximum possible increase in the computational block ia64 processors is 8 points. The outcome of the changes in calculation speed is presented in Table 2.

Table 2. Number of in/out two-step algorithms DCT and DCT algorithm based on FFT blocks of 4 and 8-point



REFERENCES

[1] Wolf W., High-Performance Embedded Computing: Architectures, Applications, and Methodologies, *Elsevier* 2007.

[2] Hsiao S.F., Shiue W.R., Tseng J.M., [34] A cost efficient fully-pipelinable architecture for DCT/IDCT, *IEEE Transactions on Consumer Electronics*, 45 (2001), No. 3, 515-525.

[3] Nikara J., Application-Specific Parallel Structures for Discrete Cosine Transform and Variable Length Decoding, *Tampere, Finland* 2004.

[4] Yatsymirskyy M., Shifted in the Time and Frequency domains Cosine and Sine Transforms Fast Algorithms with Homogeneous Structure, *Radioelectronics and Communications Systems*, [52] Allerton Press. Inc, New York Radioelektronika.

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