Application of Proteus VSM software to simulate logarithmic analog-to-digital converter with successive approximation

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Abstract - **This article is a presentation of the application of Proteus VSM software to computer simulation of the logarithmic analog-to-digital converter (LADC) with successive approximation. For the chosen parameters of converter structure, the simulation with chosen capacitance of accumulative capacitors has been conducted.**

Keywords - **analog-to-digital converter, logarithm, successive approximation, charge, simulation, accuracy**

I. INTRODUCTION

Fast development of monitoring computer systems and digital signals of information processing favored an appearance of a considerable number of various analog-to-digital converters (ADCs) which are an important element in assuring linking between digital signals and systems with real objects. It should be emphasized that information of object condition is mostly (over 90%) in analog form. Particular attention is given to ADC with logarithmic characteristic of conversion. Using a logarithm allows an effective solution of such important tasks as compression of a dynamic range of output signals, assuring a constant value of relative error of conversion, linearization of conversion characteristics and a significant increase of efficiency of digital processors. In logarithmic arithmetic, operations of multiplication, division or raising to a power come down to operations of adding, subtracting, multiplication or division through constant coefficients of appropriate data which are in logarithmic form. [1]

II. SIMULATION OF LOGARITHMIC ANALOG TO DIGITAL CONVERTER WITH SUCCESSIVE APPROXIMATION

Analysis of the logarithmic analog-to-digital converter (LADC) with successive approximation was conducted using a signal circuit running from C1 capacitor to C2 capacitor (fig.2).

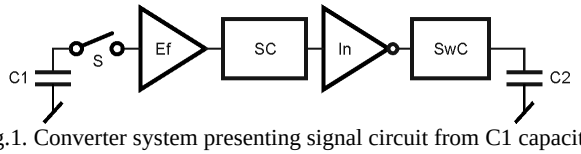

Fig.1. Converter system presenting signal circuit from C1 capacitor to C2 capacitor.

The presented system for examining the logarithmic analog-to-digital converter consists of five blocks: analog switch (S), emitter follower (Ef/Buffer), scale converter (SC) (system setting appropriate amplification lower from unity), signal inverter (In), switching circuit (SwC) (system decreasing resistance of ordinary analog switch)

Proteus Virtual System Modelling (VSM) is the simulation software which combines mixed mode SPICE circuit simulation, animated components and microprocessor models to facilitate co-simulation of complete microcontroller based designs. This software enables to develop and test such designs before a physical prototype is constructed.

This is possible because you can interact with the design using on screen indicators such as LED and LCD displays and actuators such as switches and buttons. The simulation takes place in real time (or near enough to it): a 1GMHz Pentium III can simulate a basic 8051 system clocking at over 12MHz. Proteus VSM also provides extensive debugging facilities including breakpoints, single stepping and variable display for both assembly code and high level language source. [2]

Below is presented screen shot from the simulated logarithmic analog to digital converter.

It is assumed that the LADC system works with the same capacitances on input and output (C1=C2). In the simulation of the analog-to-digital converter these capacitances were chosen considerably higher than the parasitic capacitances of the system and were equal to 10 nF. For the realization of particular blocks of the converter (fig.1) switches AD4066 and operational amplifiers AD747AP were used.

Results of the simulation are presented in fig.3 in which for time from 0 to 1 μs the converter is switched off and in time t_0 = 1 μs becomes its switching-on. Analysis is considered for the first tick of the converter, that is when the voltage reference from C1 capacitor is equal to 10V and is transferred through the scale converter (SC) on C2 capacitor. In this analyzed tick the weight of the scale converter is set to 0.1 which sets the voltage on capacitor C2 sets on 1 V. In analyzed system parasitic capacitances of LACP (which have influence on oscillations occurring on capacitor C2) have been taken into account.

These oscillations result from influence of parasitic capacitances of the system. It should be stated that with an increase of capacitance, the time of charging C2 capacitor increases and also the time of one tick of the converter increases. Obviously the time of one tick can be decreased to an appropriate acceptable error of the converter (fig.3). By using capacitances of accumulative capacitor equal to 10 nF, the frequency of oscillations on C2 capacitor does not have such a significant meaning as the lasting time of these oscillations. In fig.3 amplitude of impulse response for time

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from 8 to 14 μs has been magnified twenty times. Assuming that the scaling output voltage from C1 capacitor finishes in 11 μs then the scaled voltage on C2 capacitor will be with relative error equals δ= ±0.06.

On the output of LADC converter signal oscillations whose frequency depends on used parameters of system elements and accumulative capacitors C1 and C2 occur. From conducted simulation it can be stated that with increase of capacitance of accumulative capacitors (from 0.1 nF to 100nF) time of stabilizing response (time of fading signal oscillations on C2 capacitor) increase for the smaller accumulative capacitors from 0.1 nF and result in faster

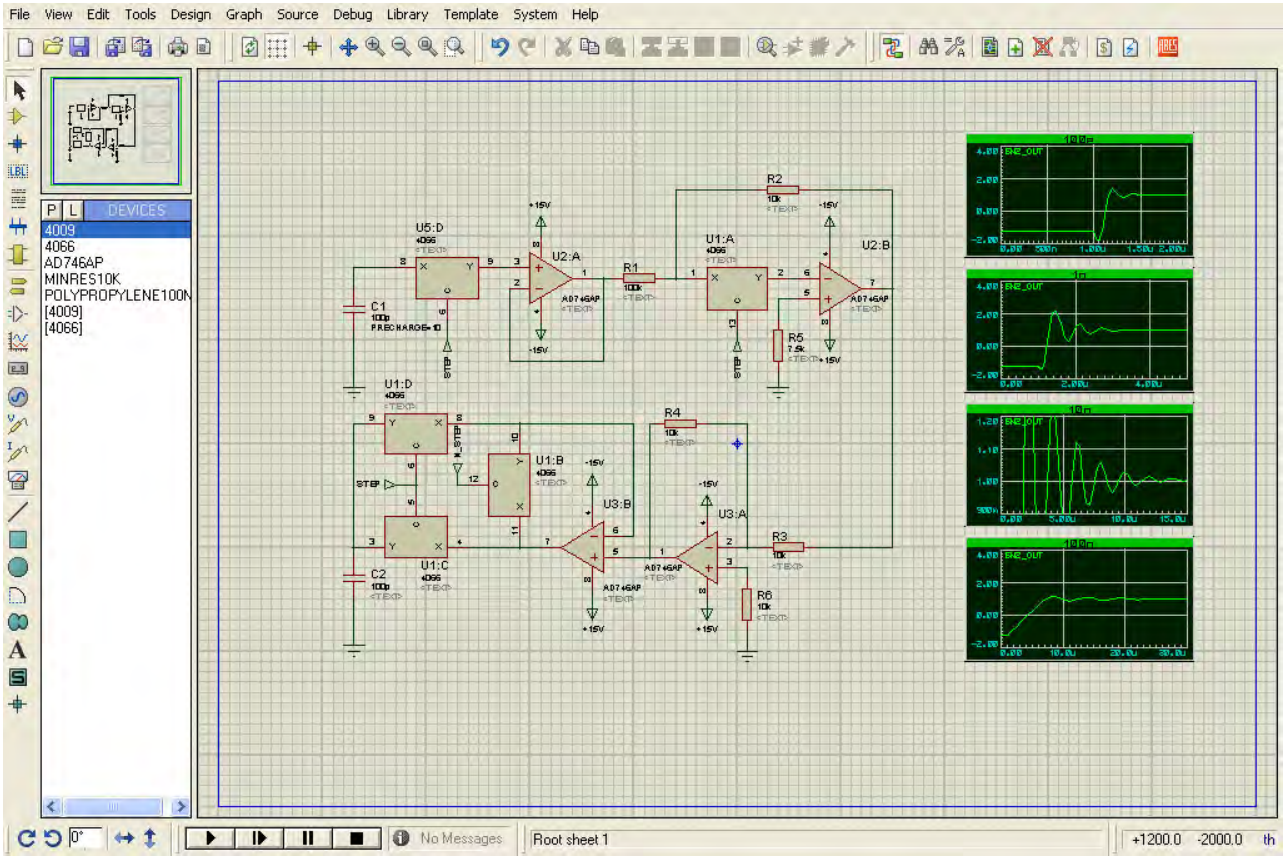

Fig.2. Simulation circuit (screen shot of the system diagram from the simulation software - Proteus)

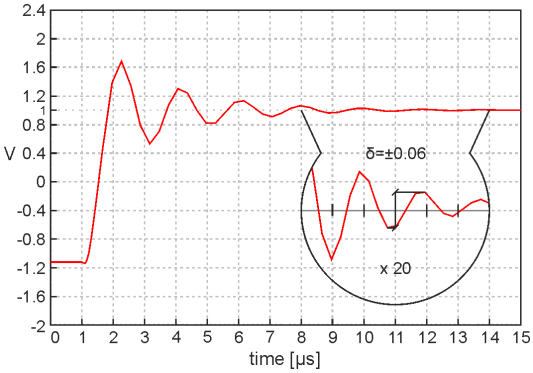

Fig.3. Voltage on C2 capacitor before and after switching-on one measuring tick of the converter for capacitances C1, C2 equal 10 nF

III. SUMMARY

On the basis of conducted analysis of the logarithmic analog-to-digital converter it can be stated that:

discharge of capacitance (lack of keeping charge) which influence the error of converter conversion.

REFERENCES

[1] Szcześniak A., Myczuda Z „A method of charge accumulation in the logarithmic analog-to-digital converter with a successive approximation”, Przegląd Elektrotechniczny (Electrical Review), ISSN 0033-2097, R.86 nr 10/2010 str.336-340

[2] http://www.labcenter.com/products/vsm_overview.cfm

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