LINEAR-MODE OPERATION OF A HIGH-ORDER SINGLE-BIT SIGMA-DELTA MODULATOR

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Abstract: This paper considers a simulation mathematical model of a high-order single-bit sigma-delta modulator. Both the condition and the criterion of this modulator operation in a linear mode have been formulated.

Key words: high-order sigma-delta modulator, linear-mode operation, simulation model.

1. Introduction

The sigma-delta modulators (SDM) are the base of most precision analog to digital converters (ADC) at the present time [1, 2]. Usually SDMs are divided to single- or malty- bit according to the capacity of output code [3]. The precision ADCs are usually based on single bit SDM [4, 5]. The single bit SDMs are divided to first- … order according to the number of feedback loops.

The structure of single bit high order SDM is presented on fig. 1. Its forward signal's line consists of the set of summators ⊗, the set of integrators ∫ and synchronous comparator SC, which consists of asynchronous comparator and synchronous D- trigger TT. The feedback loop consists of single bit digital to analog converter DAC controlled by output code of SDM. The trigger TT is synchronized by pulse generator G. The most impotent points of the SDM are signed by letters in the circle. The output code of SDM – Nx(t).
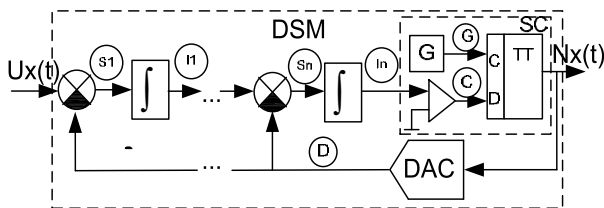

Fig. 1. Structure of a high- order single- bit SDM

The investigation of high order SDM [6] detected the problem of SDM operation in linear operating mode for input signals changing in wide dynamic range. The linear operation mode of SDM here we mean as linear operation mode of ADC based on SDM. This mode is in the condition when increasing (decreasing) of input analog voltage of SDM brings proportional increasing (decreasing) of result ща analog to digital conversion. It is caused by the fact if output signal of some integrator

exceed feedback signal the next integrator can not discharge. It is because this next integrator continues integration the same polarity signal that it was in the previous cycle. So the direction of moving of output signal of this integrator is not changed and integrator comes to saturation. It breaks the forward signal's line and fixes the output code of SDM. So the main objective of this work is in investigation of conditions of absence the described effect and providing the stable operation of high order SDM in linear operation mode.

According to the traditional conception of stability of discrete systems [7] "the limited output signal in the condition of limited input signal" the SDM is always stable because its output signal has limited number of conditions. So the indicated before condition of stability is always true. The analisys of leterature [3, 8] show that problem of providing linear operation mode for high order SDM is not indicated and it does not allow us to develop SDM, which operates in wide dynamik range.

2. Simulation model of high-order single-bit SDM

The sensitive points of SDM are marked by letters in circles in Fig.1. The voltage dependences of time t for these points can be described by a components equation of a simulation model of n-order SDM. The topology equation of the linear simulation model of n-order SDM (for $n \geq 2$) can be described by the following system of equations

$$
\begin{cases}
U_G(t) = \begin{cases} 1, t \in \left[k \times T, (k+0,5) \times T\right] \\ 0, t \in \left((k+0,5) \times T, (k+1) \times T\right) \end{cases} \\
U_C(t) = \begin{cases} 1, U_{In}(t) > 0 \\ 0, U_{In}(t) \leq 0 \end{cases} \\
U_{S1}(t) = U_X(t) - U_D(t) \\
U_{Ii}(t) = \dfrac{1}{\tau_i} \displaystyle\int_0^t U_{Si}(t)dt; i = \overline{1,n} \\
U_{Si}(t) = U_{I(i-1)}(t) - U_D(t); i = \overline{2,n} \\
N_X(t) = \begin{cases} U_C(t), (U_G(t)=1) \wedge (U_G(t - \Delta t)=0) \\ N_X(t - \Delta t) \end{cases} \\
U_D(t) = \begin{cases} E, N_X(t)=1 \\ -E, N_X(t)=0 \end{cases}
\end{cases}
, \qquad (1)
$$

where: U_X is the input voltage; N_X is the output code, which corresponds to U_X; $U_{S1}...U_{Sn},U_{I1}...$ $...U_{In},U_C,U_G,U_D$ are the voltages of the appropriate points of SDM; τ is the integrator time constant; T is the pulse generator period; k is the integer value; $\Delta t \to 0$ is the time step of modelling; E is the output voltage of DAC.

3. Linear-mode operation

The condition of n-order SDM operation in the linear mode can be presented as

$$U_{I\,MAX\,i} < E, i = \overline{1, n-1} \quad ,$$

where: $U_{I\,MAX\,i}$ is the maximum allowable output voltage of i-th integrator, which is achieved at the end of the integrating pulse when the output voltage of the previous integrator, or the input voltage for the first integrator, is maximum and of opposite polarity to the DAC's output voltage. This condition may be presented as follows

$$
\begin{cases}
U_X = U_{X\,MAX} > 0 \\
U_D = -E \\
U_{I1}(t) = \dfrac{1}{\tau_1}\displaystyle\int_0^t (U_{X\,MAX} + E)dt < E \\
U_{Ii}(t) = \dfrac{1}{\tau_i}\displaystyle\int_0^t (U_{I\,i-1} + E)dt < E; i = \overline{2, n-1}
\end{cases}
, (2)
$$

where $U_{X\,MAX}$ is the maximum allowable input voltage for the linear operating mode of SDM.

The integrals of (2) we can present as

$$\int_0^t f(t)dt = \int_{t-T}^t f(t)dt + C; \ C = \int_0^{t-T} f(t)dt \ . \ (3)$$

When we take (3) into consideration we can present (2) in such form

$$
\begin{cases}
U_{I\,MAX\,1} = \dfrac{1}{\tau_1}(U_{X\,MAX} + E)T + C_1 < E \\
U_{I\,MAX\,2} = \dfrac{1}{\tau_2}\dfrac{1}{\tau_1}(U_{X\,MAX} + E)\dfrac{T^2}{2} + \dfrac{1}{\tau_2}(C_1 + E)T + C_2 < E \\
\text{..} \\
U_{I\,MAX\,n-1} = \prod_{i=1}^{n-1}\dfrac{1}{\tau_i}(U_{X\,MAX} + E)\dfrac{T^{n-1}}{(n-1)!} + \prod_{i=2}^{n-1}\dfrac{1}{\tau_i}(C_1 + E)\times \\
\times\dfrac{T^{n-2}}{(n-2)!} + ... + (C_{n-2} + E)T + C_{n-1} < E
\end{cases}
$$

where $C_1...C_{n-1}$ is the output voltage of an appropriate integrator at the beginning of an integration cycle.

In the steady-state operation conditions the output voltages of all integrators are periodic signals with a volt-second area of charging pulses equal to an area of recharging pulses and the average value of this voltage equal to the input voltage of SDM. So, the output voltage of each integrator is not more than the input voltage at the beginning of a charging cycle

$$C_i \le U_{X\,MAX}, i = \overline{1, n-1} \quad . \quad (4)$$

Therefore, the condition of linear operating mode we can present as

$$\sum_{i=1}^{m}\left(\frac{T^{m-i+1}}{(m-i+1)!}\prod_{j=i}^{m}\frac{1}{\tau_j}\right) < \frac{1-K}{1+K}; m = \overline{1, n-1} \ , \ (5)$$

where $K = \dfrac{U_{X\,MAX}}{E}$.

At the same time the output signal of the last (n-th) integrator can be varied in the range [0, E]. This allows us to decrease the influence of comparator's parameters on ADC's error. We can present this condition so:

$$U_{In}(t) = \frac{1}{\tau_n}\int_0^t (U_{I\,n-1} + E)dt < E \ . \quad (6)$$

Taking into consideration (3) and (2) we can present (6) in the form

$$\tau_n > 2T \quad . \quad (7)$$

4. Computation of SDM's parameters

The computed parameters of 6-th order SDM are presented in Table 1 for the frequency of pulse generator 100 kHz (T=10 μS) and output voltage of DAC ± 5 V.

Table 1

Parameters of SDM

	$U_{X\,MAX} = 2,5$	$U_{X\,MAX} = 3,5$	$U_{X\,MAX} = 4,5$
$1/\tau_1$	3,33E+04	1,76E+04	5,26E+03
$1/\tau_2$	2,86E+04	1,62E+04	5,13E+03
$1/\tau_3$	2,88E+04	1,63E+04	5,13E+03
$1/\tau_4$	2,88E+04	1,63E+04	5,13E+03
$1/\tau_5$	2,88E+04	1,63E+04	5,13E+03
$1/\tau_6$	5,00E+04	5,00E+04	5,00E+04

As we can see in Table 1 and (7) the time constant of the last integrator depends only on the parameters of the pulse generator. The integrators' time constant beginning from the third integrator, or even beginning from the second one for the case $U_{X\,MAX} = 4,5\ V$, is a constant value and does not depend on the number of integrators. It can be explained by greater influence of the factorial function in the denominator of (5) in

comparison with the power function in the numerator. So, we can build SDM of arbitrary order using three or four types of integrators. The time constant of these integrators can be computed according to (5) and (7).

5. Experimental research

It has been proposed to investigate the obtained results by investigating oscillogrames of signals in the appropriate points of SDM with the integrators whose parameters correspond to Table 1. The investigation has been done using the simulation model of SDM described in [6, 9]. The signal oscillogrames of second order SDM are presented in Fig. 2. The curves of the output signal of the integrators are marked by symbols: "o" – for the first integrator (a blue line) and "+" – for the second integrator (a black line). These graphs have been constructed for the cases $U_X = U_{X\,MAX} = 2,5\ V$ and $U_X = U_{X\,MAX} = 3,5\ V$ (U_X marked by a red line using the symbol "*"). Changing the output signal of a synchronous comparator (signal $N_X(t)$ is marked by a polygonal green line using the symbol "◊") causes changing the direction of output signal for all integrators. As we can see in Fig. 2 the output signals of all integrators do not exceed the output voltage of the feedback DAC, therefore, the condition (2) is fulfilled for these cases. Besides, the output signal of the first integrator may be increased to higher values limited by some range because we consider inequality (4) for the worst case. It brings some increase in the real range of the input signal for the linear mode in comparison with the predefined one.
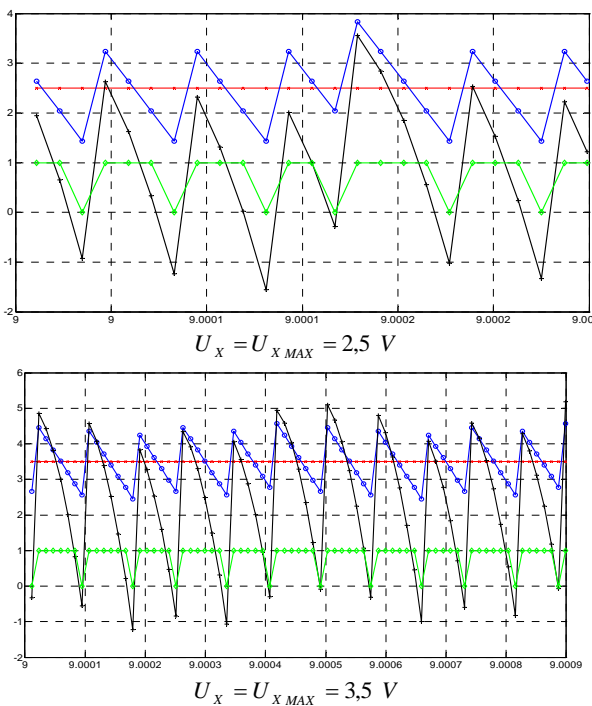
The oscillogrames of the third order SDM signals are presented in Fig. 3. The curves of the output signal of the integrators are marked by symbols: "o" – for the first integrator (a blue line), "+" – for the second and "◊"– for the third (black lines). These graphs have been also constructed for the same cases $U_X = U_{X\,MAX} = 2,5\ V$ and $U_X = U_{X\,MAX} = 3,5\ V$ (U_X marked by a red line using the symbol "*"). Similarly as it has been observed for the second order SDM, changing the output signal of a synchronous comparator (signal $N_X(t)$ is marked by a polygonal green line using the symbol «◊») causes changing the direction of output signal for all integrators. As we can see in Fig. 3 the output signals of all integrators also do not exceed the output voltage of the feedback DAC, therefore, the condition (2) is fulfilled for these cases, too. And as it has been for the second order SDM we also have some reserve for the output signal for the second and third integrators. It will also bring increasing the range of input signal for the linear mode of the whole SDM.
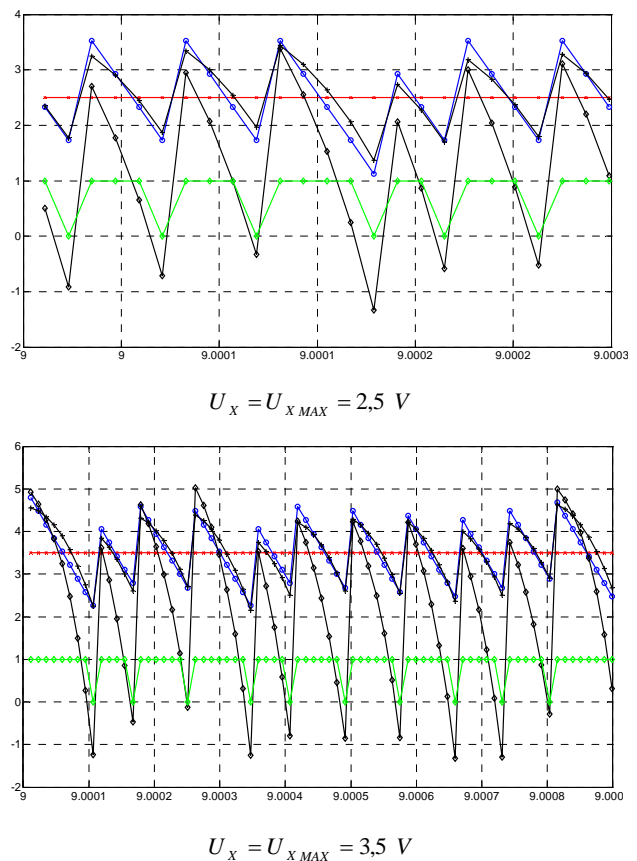

$U_X = U_{X\,MAX} = 2,5\ V$

$U_X = U_{X\,MAX} = 3,5\ V$

Fig. 3. Oscillogrames of third order SDM

$U_X = U_{X\,MAX} = 2,5\ V$

$U_X = U_{X\,MAX} = 3,5\ V$

Fig. 2. Oscillogrames of second order SDM

Simulation of a higher-order SDM proves self-oscillating of integrator's output signals. These oscillations could be explained by transformation of the

negative feedback to a positive one when we have four and more series-connected integrators. This problem can be solved by introducing nonlinear components or nonlinear connection into the structure of the higher-order SDM or by changing the structure of SDM to high-order cascade [3], which includes a set of series-parallel connected first-, second- or third- order sub-modulators.

6. Conclusions

Therefore, there has been conducted the analysis of the simulation mathematical model of a high-order single-bit sigma-delta modulator which allows us to formulate the condition and to obtain the criterion of its operation in the linear mode. Also the presented apparatus enables to compute the parameters of integrators for SDM, which operates in the linear operating mode for the defined range of input signals. The simulation of second and third order SDM operation confirms the linear mode for input signal changing in the predefined range for parameters of SDM computed by the presented methodology.

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ЛІНІЙНИЙ РЕЖИМ РОБОТИ ОДНОБІТНОГО СИГМА-ДЕЛЬТА МОДУЛЯТОРА ВИСОКОГО ПОРЯДКУ

Р. Кочан

Розглянуто імітаційну математичну модель однобітного сигма-дельта модулятора високого порядку.

Сформульовано умову та критерій роботи цього модулятора в лінійному режимі.

Roman Kochan – Ph.D. in information measurement systems, an associate professor of Specialized Computer Systems Department. Research interests: DAQ System and Network, Intelligent Measurement Systems.