The Approaches to Reduction Power Consumption in Integrated Circuits

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Abstract – **During the development of information society and technology portable hand-held electronic devices are increasingly enter in everyday life. Trends toward continuous growth of these devices complexity and, therefore, increase the need for providing them with enough energy are obvious. The approaches to reduce power consumption in integrated circuits are studied in the paper.**

Keywords –**power consumption, energy harvesting.**

I. INTRODUCTION

Relevance of developing methods for designing microelectronic digital devices with low power consumption can be defined by the following main factors:

- presence of multiple applications, which must combine high reliability and the required performance with low power consumption for a given battery life;
- the need of reducing power consumption to address the problem of heat removal, as it determines the weight and size parameters of devices;

II. WAYS TO MINIMIZE POWER CONSUMPTION IN ICS

For today's digital circuits consumption is divided into two components: static and dynamic:

$$P_{total} = P_{dyn} + P_{leakage} \quad (1)$$

The dynamic energy of synchronous digital circuit is determined by the following equation:

$$P_{dyn} = a * f * \frac{1}{2} C_L V_{DD}^2 \quad (2)$$

Where a is activity (average number of transitions per clock cycle (clock has two); f – frequency; C_L – switched capacitance; V_{DD} – supply voltage.

Reduction in dynamic consumption is possible by reducing the parameters of the Eq. (2).

Reducing activity is possible with Clock Gating [1] and Data Gating methods.

To reduce switched capacitance *C* the following conditions are needed to consider:

- Careful transistor sizing (small transistors off critical path);
- Tighter layout (good floor planning);

Reducing frequency doesn't save energy, just reduces rate at which it is consumed (lower power, but must run longer).

According to Eq. (2) reducing supply voltage is most effective because it leads to a quadratic reduction in energy consumption.

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Static consumption is mainly conditioned by the gate leakage current. Under ideal scaling, want to reduce threshold voltage as fast as supply voltage, but subthreshold leakage is an exponential function of threshold voltage and temperature

$$I_{leakage} \approx e^{\frac{V_T}{T}} \quad (3)$$

Run-time leakage reduction is possible by using Power Gating [2] method.

III. ENERGY EFFECTIVE METHODS APPROBATION

To evaluate the effectiveness of the methods described in section II, it was decided to investigate their effect on consumption of models of digital circuits. Research was carried out using CAD tool Advanced Design System (ADS). The circuit was built on CMOS transistors.

To analyze the effect of clock frequency and supply voltage on the circuit's power consumption Clock Gating, Data Gating and Power Gating techniques was used. Energy efficiency of the applied methods was calculated by the following equation:

$$Eef = 100\% - \frac{P_N}{P_O} \cdot 100\% \quad (4)$$

Where P_N – average consumption after changes; P_O – average consumption before changes.

The simulation results show that the effectiveness of techniques that were mentioned above exceeds 50%. To approbate the simulation results it was decided to design the benchmark circuit similar to the model. The results of power consumption measurement of a real device and the device model have matched.

IV. CONCLUSION

All described methods can significantly reduce the power consumption of the circuit. The most effective methods are: supply voltage scaling and Power Gating, which allow to achieve more than 60% increase in energy efficiency.

REFERENCES

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