

# Verification System for SoC HDL-code

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**Abstract** – Assertion-based models and methods for the verification and diagnosis of HDL-code functional failures, which make possible to reduce considerably time-to-market of software and hardware, are developed.

**Keywords** – testing, verification, HDL-model, Infrastructure IP.

## I. INTRODUCTION

A new model of software in the form of Code-Flow Transaction Graph, as well as a new matrix method for diagnosing functional failures, which are characterized by adaptability of data preparation when detecting faulty blocks, are proposed. Methods for searching functional failures, which differ in parallel execution of vector operations on the rows of a functional failure table, are improved. They allow substantially (x10) increasing the performance of computational procedures associated with diagnosis and repair of software and hardware.

## II. IMPLEMENTATION OF MODELS AND METHODS IN THE VERIFICATION SYSTEM

Practical implementation of assertion-based models and methods for testing and verification is integrated into the simulation environment Riviera of Aldec Inc., Fig. 1. New assertion and diagnosis modules, added in the system, improved the existing verification process, which allowed 15% reduction the design time of digital product.

Actually, application of assertions makes possible to decrease the length of test-bench code and considerably reduce (x3) the design time (Fig. 2), which is the most

values of all internal signals is appeared. This allows quickly identifying the location and type of the functional failure, as well as reducing the time of error detection in the evolution of product with top-down design. Application of assertion for 50 real-life designs (from 5 thousand up to 5 million gates) allowed obtaining hundreds of dedicated solutions, included in the verification template library VTL, which generalizes the most popular on the market EDA (Electronic Design Automation) temporal verification limitations for the broad class of digital products. Software implementation of the proposed system for analyzing assertions and diagnosing HDL-code is part of a multifunctional integrated environment Aldec Riviera for simulation and verification of HDL-models. High performance and technological combination of assertion analysis system and HDL-simulator of Aldec company is largely achieved through integration with the internal simulator components, including HDL-language compilers. Processing the results of the assertion analysis system is provided by a set of visual tools of Riviera environment to facilitate the diagnosis and removal of functional failures. The assertion analysis model can also be implemented in hardware with certain constraints on a subset of the supported language structures. Products Riviera including the components of assertion temporal verification, which allow improving the design quality for 3-5%, currently, occupies a leading position in the world IT market with the number of installations of 5,000 a year in 200 companies and universities in more than 20 countries on the world.

## III. CONCLUSION

The infrastructure for verification and diagnosis of HDL-code for design digital systems-on-chips, which involves four process models for testing, diagnosing, optimization and correcting errors, closed in a cycle, that makes it possible to reduce the time of code debugging, when creating a design. Practical implementation of models and verification methods is integrated into the simulating environment Riviera of Aldec Inc. New assertion and diagnosis modules improved the existing verification process, which allowed 15% reduction in overall design time of digital products.

## REFERENCES

- [1] M.F. Bondaryenko, O.A. Guz, V.I. Hahanov, Yu.P. Shabanov-Kushnaryenko, "Infrastructure for brain-like computing," *Kharkov: Novoye Slovo*, 160 p., 2010.
- [2] R. Ubar, S. Kostin, J. Raik, "Embedded diagnosis in digital systems," *26th International Conference "Microelectronics", MIEL 2008*, pp. 421-424, 2008.
- [3] E.J. Marinissen, Yervant Zorian, "Guest Editors' Introduction: The Status of IEEE Std 1500," *IEEE Design & Test of Computers*, No26(1), pp.6-7, 2009.

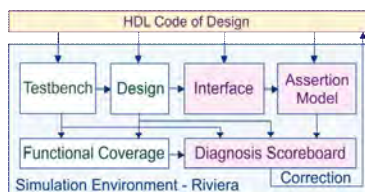


Fig. 1. Implementation of results in the system Riviera

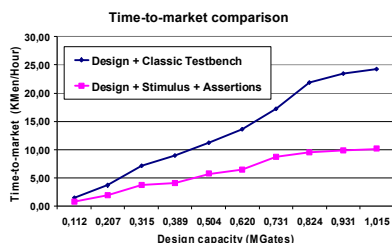


Fig. 2. Comparative analysis of verification methods

expensive [1-3]. Assertion engine allows increasing the diagnosis depth of functional failures in software blocks up to level 10-20 HDL-code statements. Due to the interaction of simulation tools and assertion engine, automatically placed inside the HDL-code, an access of diagnosis tools to the