FPGA Based Control System with Reconfigurable Coprocessor

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Abstract – **In this paper proposed structure of reconfigurable processor system based on the COTS components and open source tools**

Keywords – **Reconfigurable processor, Leon, open source platform**

I. INTRODUCTION

There are a lot of approaches for developing specialized reconfigurable systems with different benefits, like speedup calculation process, more robust systems, e.t.c. But mostly authors don't observe the system in complexity of overall developing process, like compiler, possibility and complexity of writing software, architecture for software developers. In proposed system was decided to use a commercial of the shelf hardware components and open source software components

II. SYSTEM DESCRIPTION

As the main market for such system is the space, we mustn't use any netlists or precompiled library, all code must be present in the text form. That's why was decided to use open source Leon processor for this design. This processor has advantages comparatively with others FPGA processors like : high performance, free open source tools for developers (tools for configuration, toolbox for gcc use) and open VHDL code.

Structure of the processor present at figure 1.

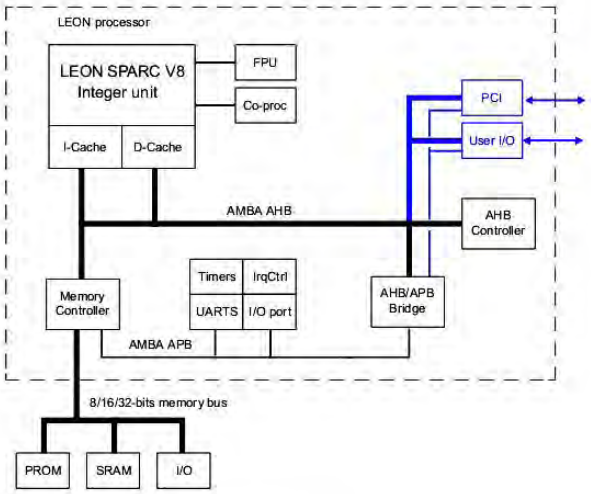

Figure 1: LEON block diagram

This processor was specially adopted for use in hard tolerant systems. For some kind of algorithms performance can be enhanced by using special coprocessor. But the problem is, that this part of the system is sensitive to the Single event upset. In this paper proposed to use partial reconfiguration techniques for robust design of coprocessor and special module of control for it.

For some algorithms there is a possibility to build control module with much less complexity than calculation module, but he can detect error in the calculation of main module. This module differs for different problems, and one coprocessor can have few different versions of this modules, with different complexity, and probability of error detection. That's why proposed to partially reconfigure not only the coprocessor, but also a control module.

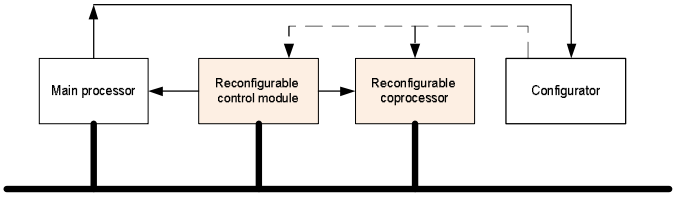

Fig.2 System structure

On the figure 2 proposed the structure of the system. Coprocessor connects to the main processor via special interface, and connects to the AHB bus. Reconfigurable control module checks the result of coprocessors operation. Configurator manages the partial reconfiguration process, and start partial reconfiguration, when command received from main processor.

III. CONCLUSION

In this paper was proposed a reconfigurable system based on FPGA software processor.

Proposed system has the following benefits:

- Modern FPGA partial configuration time is so low, that this system can make overall performance increase because of using coprocessor
- System flexibility is achieved and developing time decrease
- Building a system based on ready components provide less errors and decrease system developing and testing time
- Using of partial reconfiguration makes coprocessor tolerant to the SEU

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