Method and Dedicated Processor for Image Coding based on Residue Number System

Su Jun, Zhengbing Hu

Abstract - **A dedicated processor for image coding and transfer in wireless networks was developed on the basis of the residue number system. Received residues are transferred by parallel channels using multipath routing. Selected co-prime modules provide conversion of the 24-bit images. The one pixel of image transformation is carried out once per a cycle using parallel-serial multi-bit adders and incomplete encoders.**

Keywords - **Co-processors, Image coding, Residue number system, Wireless networks, Multipath routing.**

I. INTRODUCTION

An integration of low-power wireless network technologies with an inexpensive hardware such as CMOS cameras and microphones currently contributes to the development of wireless multimedia sensor networks (Wireless Multimedia Sensor Network - WMSN). It allows a transfer of video and audio streams, stationary object images and scalar sensor data [1]. Multimedia data are characterized by a significant size of information and sensitivity to the transfer delay.

Taking into consideration functional limitations of the wireless sensors (transmission speed, computing power, self-power, etc.), an urgent task of multimedia data transfer is set to reduce the load upon the nodes-repeaters and time of the message delivery.

For an effective usage of the whole bandwidth of communication channels the authors offer such type of WMSNs, which splits multimedia data into parts and transfers them by different routes [2].

II. IMAGE CODING METHOD

It is proposed by the author to use the Chinese remainder theorem [3] as an algorithm for splitting the images. The splitting of the message is carried out using the following formula:

$$b_i = A \,(\mathrm{mod}\, p_i)\,,$$

where A – is an image for splitting, p_i – co-prime modules.

Co-prime modules are chosen from the condition $p_i < p_{i+1}$.

Image recovering (decryption) is carried out using the formula [3]:

$$A = \left(\sum_{i=1}^{n} b_i \cdot B_i \right) \mathrm{mod}\, \wp\,,$$

where $\wp = \prod_{i=1}^{n} p_i$, B_i - orthogonal basis, n - number of modules.

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$$B_i = \frac{\wp}{p_i} \cdot d_i \equiv 1 (\mathrm{mod}\, p_i)\,,\ i = \overline{1, n}\,,$$

where $1 \le d_i \le p_i - 1$ - the weight of the orthogonal elements.

Let's take, for example, the image coding (Fig. 1). The value of modules is chosen according to the rule, which predicts that the modules should be bigger than the maximum pixel value. Most video sensors use 24-bit binary code to represent a single pixel of the image. In the 24-bit representation, the maximum decimal value is 2^{24}. Therefore to convert one pixel into the residue number system were selected the following modules $p_1 = 7$, $p_2 = 23$, $p_3 = 29$, $p_4 = 59$, $p_5 = 61$, whose product is $\wp = 16803731$. Using provided modules, the n - bit numbers, where $n = \log_2 (\prod_1^5 p_i)$, can be presented.

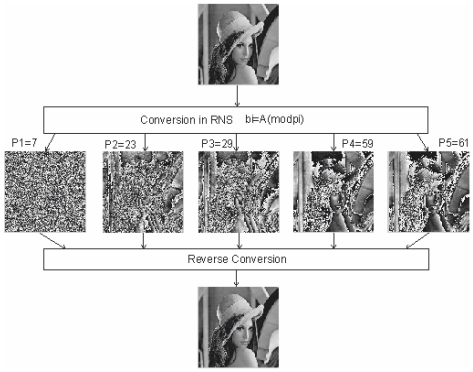

Fig. 1 Decomposition of the image by modules: 7, 23, 29, 59, 61

Conversion of a 24-bit binary code into the residue number system was implemented using the method of direct addition [4]:

$$A = \sum_{j=0}^{k} a_j \cdot 2^j \equiv b_i (\mathrm{mod}\, p_i) = \left(\sum_{j=0}^{k} a_{ij} \right) \mathrm{mod}\, p_i\,,$$

where $k -$ the number of binary digits,

$$a_{ij} \equiv \left(a_j \cdot 2^j \right) \mathrm{mod}\, p_i\,,\ a_{ij} = 0 (\mathrm{mod}\, p_i),\ \text{when}\ a_j = 0\,,$$

$$a_{ij} = 2^j (\mathrm{mod}\, p_i)\,,\ \text{when}\ a_j = 1\,.$$

III. DEDICATED PROCESSOR IMPLEMENTATION

Splitting the image into parts by modules $p_1 = 7$ $p_2 = 23$ $p_3 = 29$ $p_4 = 59$ $p_5 = 61$ is implemented as a separate

co-processor. Image binary code (24 bit) is entered to the input register RG. The information that was read from the registry is entered to the encoder inputs (EC1 - EC5). When "1' is present in the register place n then a binary code that corresponds to the coefficients according to Table 1 is formed at the encoder output. The binary code enters from the encoder outputs to the adders by base p_i inputs (AD).

The encoder work for module $p_1 = 7$ is described by the following logical equations:

$$f_{p1\_0}[0] = E0 \wedge a_0;$$

$$f_{p1\_1}[1..0] = E0 \wedge (a_1 \vee a_0);$$

$$f_{p1\_2}[2..0] = E0 \wedge (a_2 \vee a_1 \vee a_0),$$

where a_0, a_1, a_2 - the bits coefficients; E0 – enabling input, when $E0 = 1$ a code is formed in the encoder output according to Table 1.

A multi-digit parallel-serial adder was developed by modules p_i ($i = 1,..,5$) to reduce the conversion time of 24-bit binary numbers into the residue number system code (Fig. 2).

The complexity of logic equations writing has considerably increased along with the increase of the module number of bits, therefore the work of adders by modules $p_1 = 7$, $p_2 = 23$, $p_3 = 29$ $p_4 = 59$, $p_5 = 61$ can be described using VHDL.

A verification of the dedicated processor developed at Quartus II software of Altera Corporation confirmed its correct work

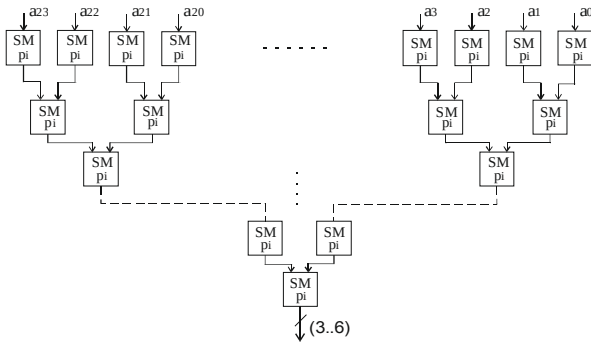

Fig. 2 Block diagram of multi-digit adder by module p_i : $a_0 \div a_{23}$ - coefficients of expression $a_{ij} = 2^j \bmod p_i$ (see Table 1).

The developed dedicated processor for image coding using the residue number system provides high performance while using incomplete encoders and parallel-sequential multi-digit adder by the relevant modules. Dedicated processor is implemented by CPLD series MAX-II of ALTERA Corporation, chip EPM240T100C5, conversion time of 24-bit binary code (one pixel) is 16.7 ns, respectively the transformation of one image frame (640*480) equals approximately to 5 ms.

The obtained images (residual) b_i are transmitted by different routes basing on multipath routing protocol.

Table 1

COEFFICIENTS GENERATED BY AN ENCODER, WHEN A SINGLE INFORMATION BIT IS ENTERED ON INPUT

mod	$2^j (\bmod p_i)$													
	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}		2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
mod 7	4	2	1	4	2	…	2	1	4	2	1	4	2	1
mod 23	2	1	12	6	3	…	13	18	9	16	8	4	2	1
mod 29	10	5	17	23	26	…	12	6	3	16	8	4	2	1
mod 59	47	53	56	28	14	…	10	5	32	16	8	4	2	1
mod 61	10	5	33	47	54	…	6	3	32	16	8	4	2	1

IV. CONCLUSIONS

The image splitting into parts in residue number system and usage of multipath routing in the wireless sensor networks allow reducing the load on the nodes-repeaters and reduce the time of the message delivering up to 2-3 times, depending on the number of independent routes. In case that the message is splitting into the parts of different capacity (in illustrated example $3 \div 6$ bits), its transferring can be done with route bandwidth and reliability allowance. The developed dedicated processor transforms one pixel of the image per one cycle, while the transformation of one image frame (640*480) need approximately 5 ms.

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