Express Method of Threshold Voltage Control of DMOS Transistors in the Process of their Manufacturing

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Abstract – **There is shown the use of test structure for DMOS-structure threshold voltage control and correction.**

Keywords - **DMOS Transistors, Threshold Voltage.**

I. Introduction

Structural peculiarity of DMOS transistors is formation of *p*-area, which serves as its substrate (*p*-channel area), by method of boron impurity redistribution from the finite source formed by ion-implantation doping method.

Such method of forming *p*-channel area of the structure has some advantages, as unlike forming the channel, it makes impossible the formation of structures with the channel length less than 1 micrometer. At the same time, there arises a problem of controlling the threshold voltage of DMOS structures because of its dependence on the coordinate of the channel local region.

II. Problem Statement

The paper proposes an express method of DMOS transistor threshold voltage control with the help of test structure which is a compressed resistor, formed by boron impurity diffusion profile (*p*-channel area) and phosphorus (drain of the transistor) (fig.1).

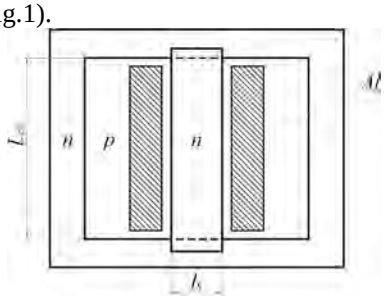

Fig.1. Test structure for DMOS-transistor threshold voltage control

Considering distribution profiles of phosphorus and boron impurities to be near to exponent, we can write down the following relation with the resistance of the compressed resistor $R_{c.r.}$

$$R_{c.r.} = \frac{1}{0.85 \cdot q \cdot m_p(x_{so}) L_a N_a(x_{so})}, \qquad (1)$$

where $m_p(x_{so})$ – hole mobility in the points of metallurgic *p-n*-junction, L_a – characteristic length of boron impurities in *p*-channel area, $N_a(x_{so})$ – boron impurities concentration value in the point of metallurgic *p-n*-junction.

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Value of transistor activation voltage is defined by a maximum value of the resulting concentration in the *p*-channel area of the structure

$$U_{th} = j_{ms} + 2\frac{kT}{q}\ln\frac{N_{\text{a.p.}}(x_m)}{n_i} - \\ -\frac{Q_{ox}}{C_{ox}} + \frac{2}{C_{ox}}\sqrt{e_{si}e_o N_{\text{a.p.}}(x_m)\left|\frac{kT}{q}\ln\frac{N_{\text{a.p.}}(x_m)}{n_i}\right|} \qquad (2)$$

where j_{ms} - difference between operations of electron liberation from the gate and semiconductor substrate of *n*-channel MOS transistor, kT/q – temperature voltage, $N_{a.p.}(x_m)$ – boron impurities concentration maximum value in p-channel area, n_i – proper carrier concentration in Si, Q_{ox} – charge density on interface $Si-SiO_2$, C_{ox} – specific capacity of gate dielectric, e_{si}, e_o – dielectric silicon and vacuum constant respectively.

Thus, there is a correlation dependence between the values $R_{c.r.}$ and U_{th} which, according to the measured values of $R_{c.r.}$, allows to estimate DMOS structure activation voltage.

Fig. 2 shows the estimated and experimental values of U_{th} from $R_{c.r.}$.

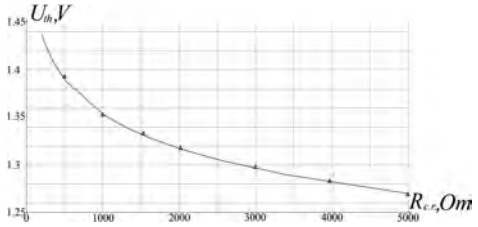

Fig.2. Dependence diagram of U_{th} on $R_{c.r.}$

On the basis of the established dependences it is possible to correct the value of U_{th} by means of doping the *p*-channel area with boron ions.

III. Conclusion

The use of a test structure as a compressed resistor enables to correct transistor unblanking voltage by means of *p*-channel area doping with gate boron ions and contact to the source region.

References

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