Multimatrix Processor for Cyberspace Analysis

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Abstract – **The structural model of high-speed multimatrix processor designed for fast and accurate search of information objects in cyberspace is described is proposed. It enables to increase considerably (x10) the speed of diagnosing single and/or multiple faults.**

Keywords – **testing, verification, HDL-model, Infrastructure IP.**

1. INTRODUCTION

Purpose of this article is creation of the individual and virtual computer in cyberspace for intelligence transactions of data and services, focused on each person [1]. The problems are: 1) Defining the functional infrastructure for virtual PCC. 2) Creating a structured database for storing information and services. 3) Developing a PCC template as a set of related services and tools focused to the needs of the user. 4) Developing a system for protection of personal cyberspace, data and services, including authentication, keys, digital signature, cryptography. 5) Creating intelligent tools for searching, pattern recognition and decision making as a set of filters, focused to a specific user. 6) Developing PCC prototype and its testing for different kinds of users.

II. ENGINE FOR CYBERSPACE ANALYSIS

For high-speed navigation in cyberspace (searching objects and evaluating their interaction) it is needed a simple and fast multimatrix processor (MMP), where each operation (and, or, xor, slc) processes in parallel and very fast only one binary operation on the matrices (two-dimensional data arrays). The number of instruction-oriented primitive matrices creates a system – heterogeneous multimatrix processor of binary operations with the buffer M, Fig. 1. Multimatrix processor module involves 4 memory blocks with built-in instructions (A – and, B – xor, C – slc – shift left crowding, D – or) and buffer memory M. The module is focused on the parallel execution in this case one of four instructions (ISA – Instruction Set Architecture) by using matrices of binary data of the same dimension $M = M\{\text{and}, \text{or}, \text{xor}, \text{slc}\}\{A, B, C, D\}$ and saves the result in the buffer M. MMP feature that is not the matrix cell has the command system of the four instructions, and each instruction has its own cell matrix as the data for parallel processing, which significantly simplifies the control structure and the whole device. The MMP complexity is moved on the data structure, where the matrix memory has a single hardware-implemented built-in instruction that allows realizing a primitive control system for parallel computing processes (SIMD – Single Instruction Multiple Data), which is sequential in nature, and therefore there is no need to create a super complex compilers, focused on parallelization of computational processes. Here, each matrix processor executes a single operation, built-in storage elements of the matrix. But there are situations, when the matrix level (M-level) of data definition is redundant to perform operations on Boolean (B-level) or registration (R-level) variables. For such case, it is necessary to have the hierarchy of data levels. The typical MMP blocks are: memory for data (DM) and programs (PM), control unit (CU), interface (I-face) and Infrastructure IP (I-IP), as well as multimatrix processor module, which includes 4 memory blocks with built-in operations (A – and, B – xor, C – or, D – slc – shift left crowding) and buffer memory M.

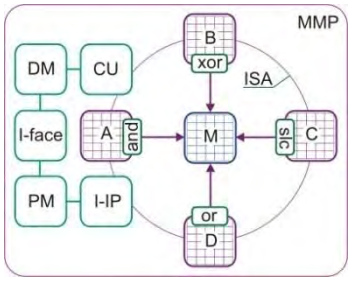

Fig 1. Multimatrix processor of binary operations

The applications of vector-logic or matrix technology for analyzing the processes or phenomena: 1) text recognition in the entry registration cards; 2) personal identification by photographs, close to the standard images for visa documents; 3) search of analogs in the Internet by the given patterns; 4) sorting images in the database according to the classes and attributes; 5) fingerprinting and creation of classified intelligence library; 6) recognition and classification of software viruses; 7) identification of targets and moving objects (aircraft, ships, cars); 8) control robotic systems; 9) pattern recognition for smell, taste, sound, heat and radio frequency; 10) recognition of linguistic structures and primitives, and their estimation when comparing with benchmarks.

III. CONCLUSION

The architecture of multimatrix processor, focused to improve the performance of decision-making in the library space, is proposed. It is characterized by using parallel logic vector operations and, or, xor, slc, which makes it possible to improve significantly (x10) the performance of functionality synthesis. The model for synthesizing functionality of a digital system in the form of multitree and method of traversal the tree nodes, implemented in the engine to search a solution of given depth, which greatly increases the performance of software and hardware design, are presented.

REFERENCES

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